

LONGBEACH 10/20

LA-2371 REV

1.0 Schematic

Portability Prescott/Northwood
RC300ML(RX300ML)+IXP150+ATI M11P(128MB VRAM)
2004-07-23

Compal Electronics, Inc.

Title

Size

Custom

Document Number

LA-2371

Rev

1.0

Date: 星期二, 七月 27, 2004

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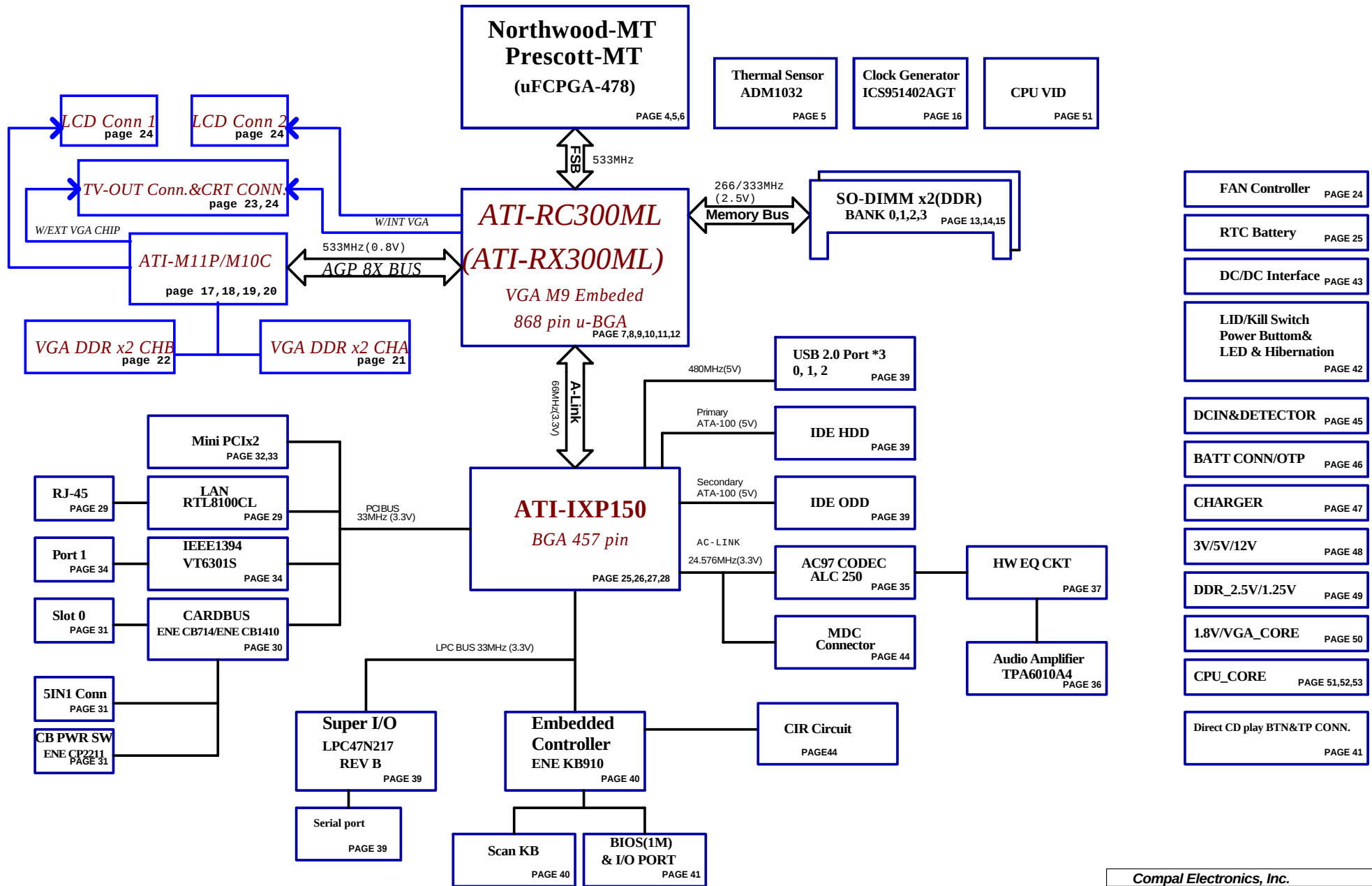
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Compal confidential

Model Name : EFQ00 & EEQ00

File Name : LA-2371 Rev: 1.0

BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X/8X	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts
VGA	AD16		PIRQA
CardBus	AD20	2	PIRQA
LAN	AD19	3	PIRQD
Mini-PCI1	AD18	1(for Wireless Lan)	PIRQC/PIRQD
1394	AD16	0	PIRQA
5IN1	AD20	2	PIRQB
Mini-PCI2	AD22	4(for TV tuner)	PIRQC/PIRQD

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b		
(24C84)	1011 000Xb		

EC SM Bus2 address

IXP150 SM Bus address

Device	Address
Clock Generator (1CS951482A6T)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 001Xb

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

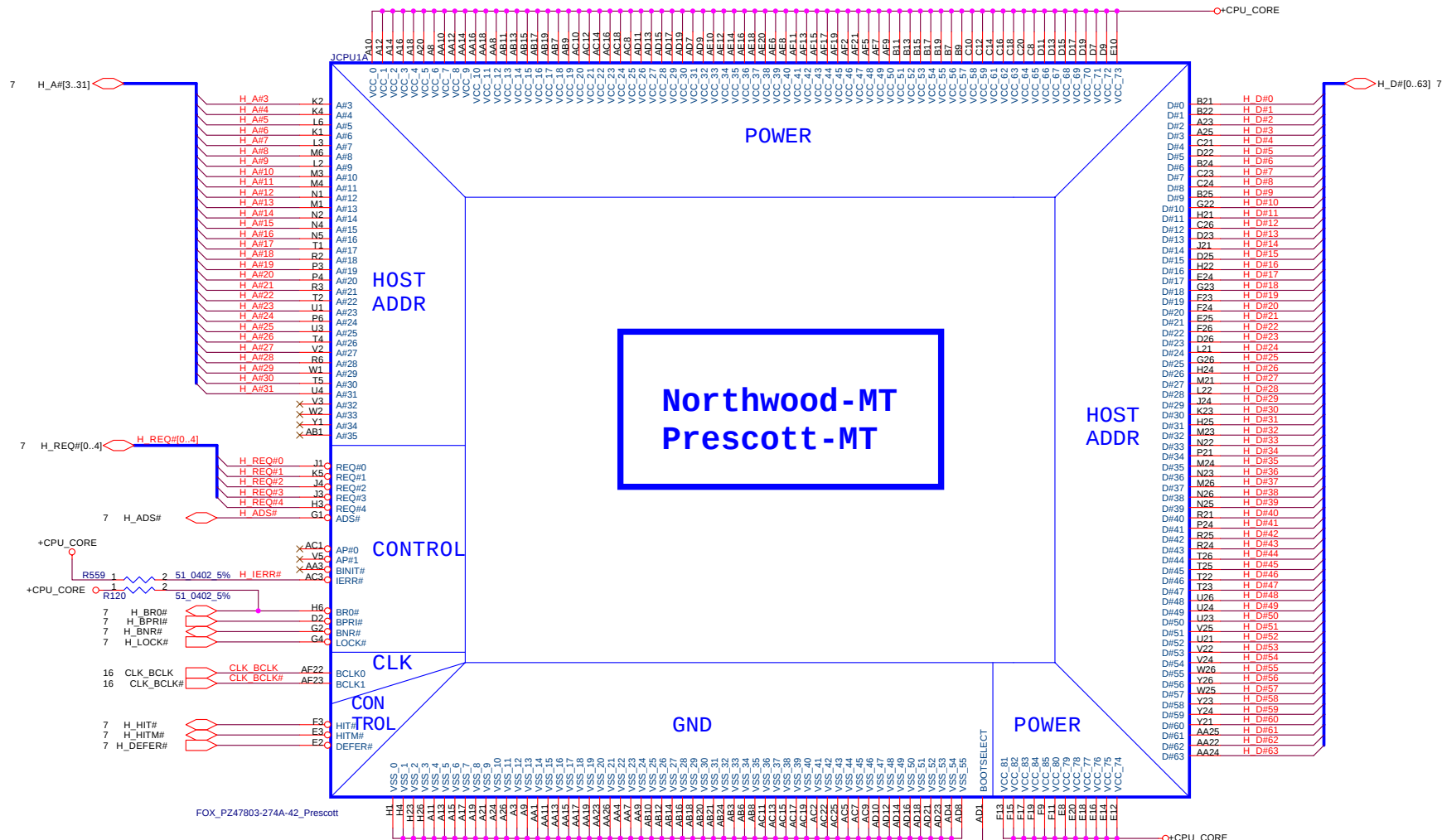
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table for AD channel

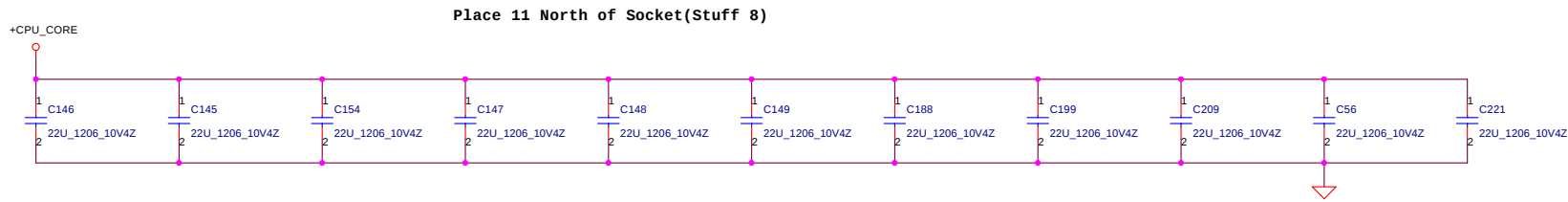
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
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7	NC	2.500 V	3.300 V	3.300 V

BIOS_ID: H EFW00
L EEW00

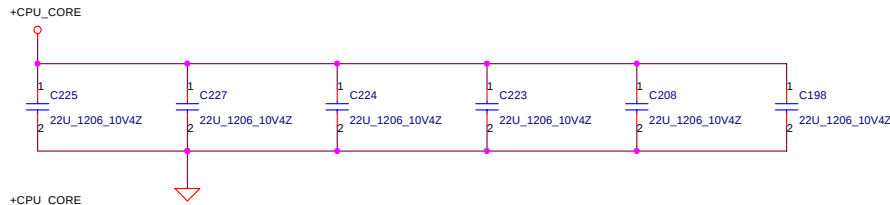
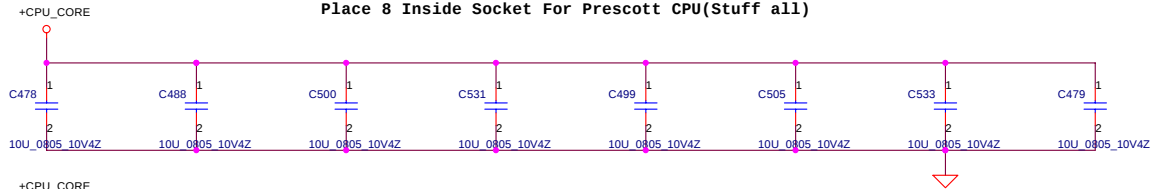
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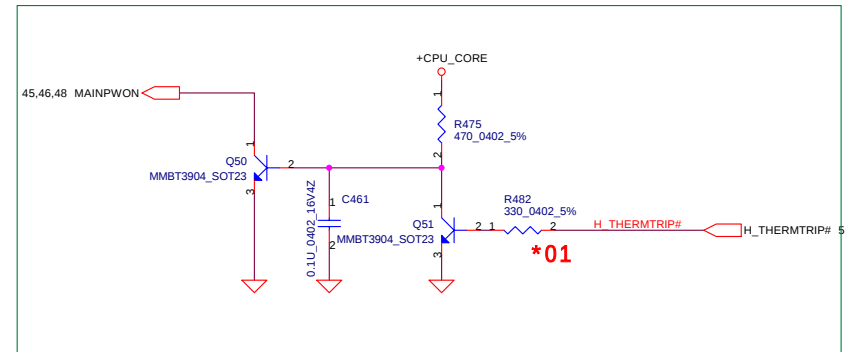
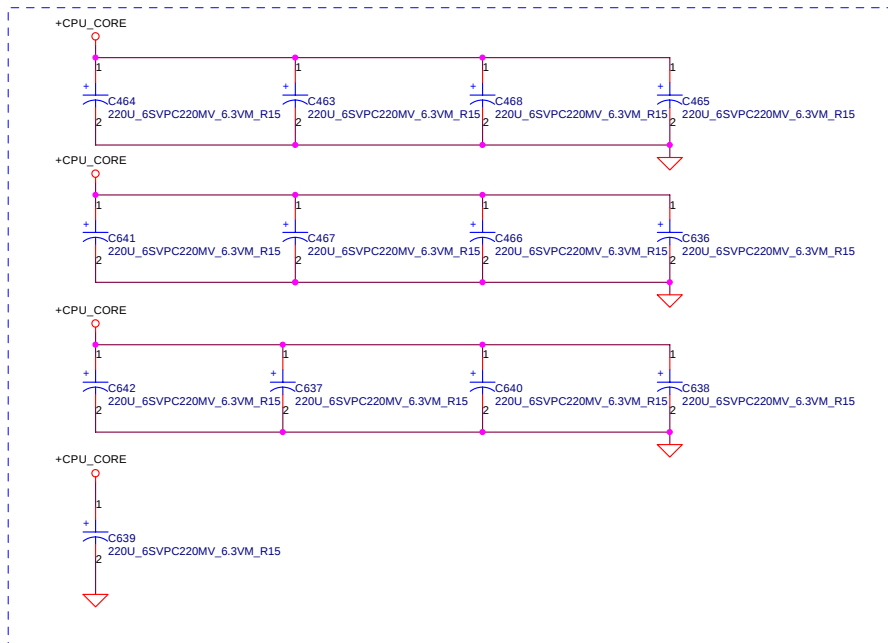


22uF depop reference
Springdale Customer Schematic R1.2 page82



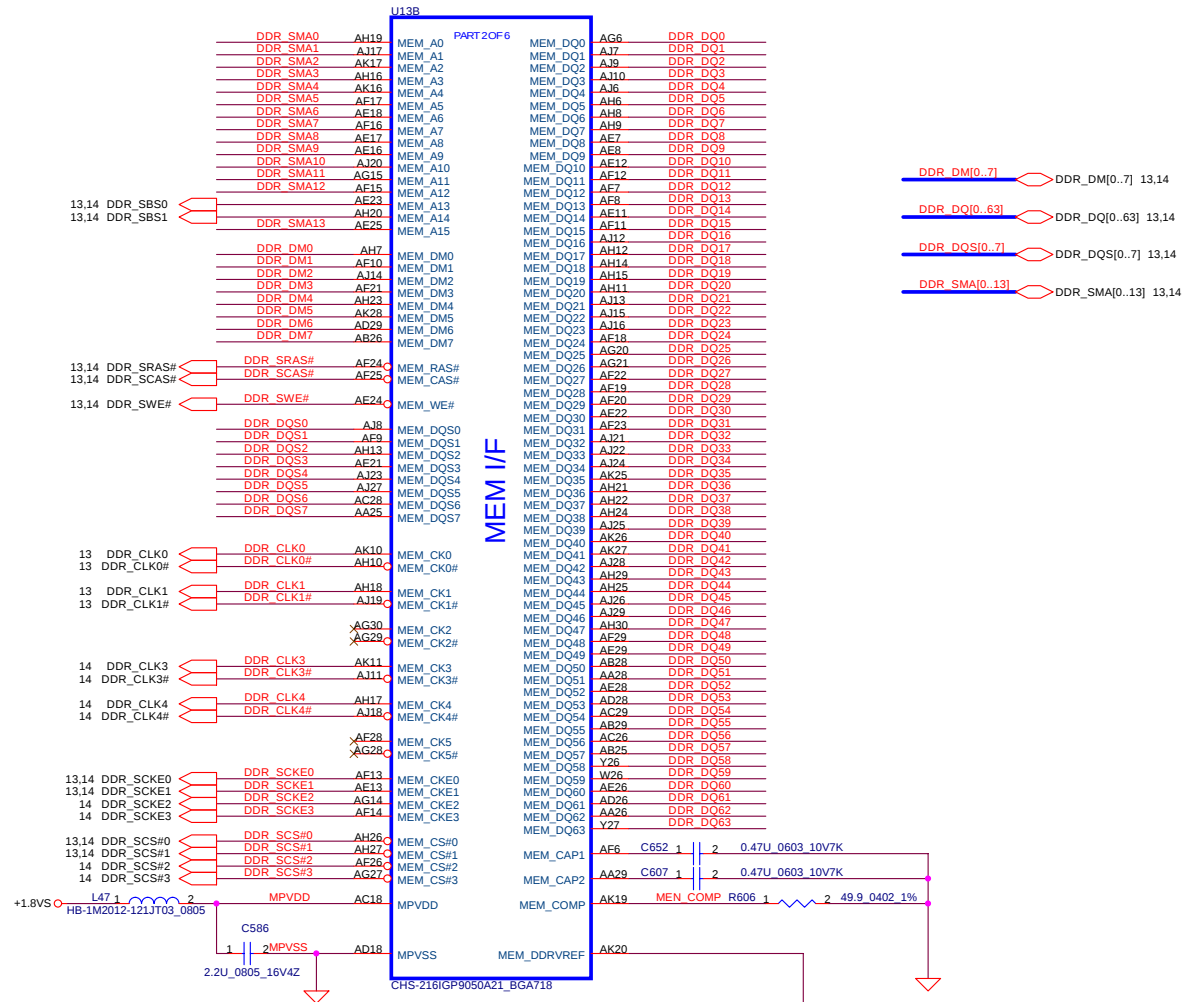
Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page239

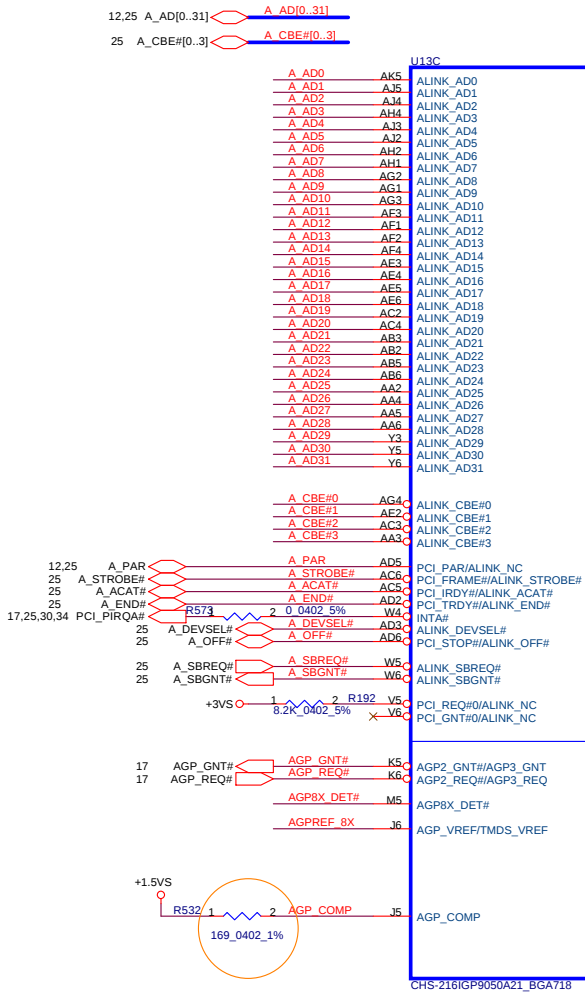
Decoupling Reference Requirement:
560uF Polymer, ESR:5m ohm(each) * 10
22uF X5R * 32



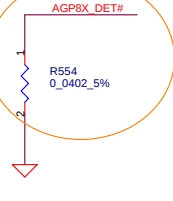
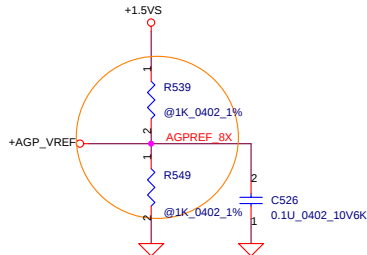
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Title		CPU Decoupling	
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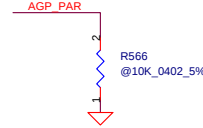




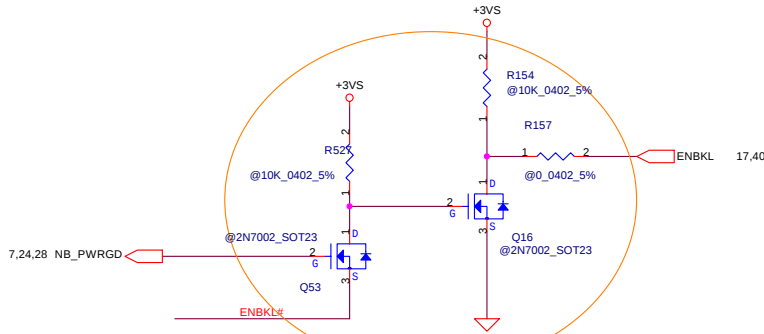
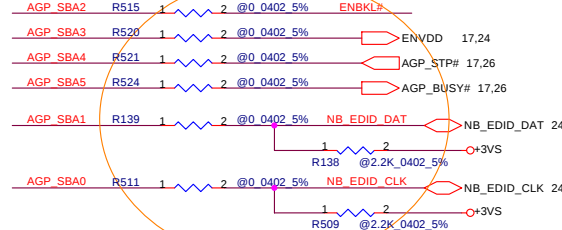
POP For EFQ00
DEPOP For EEQ00

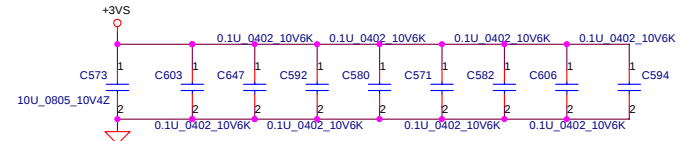
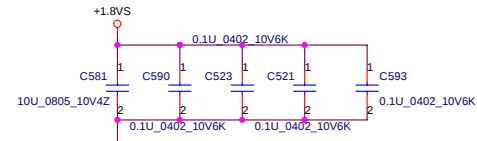
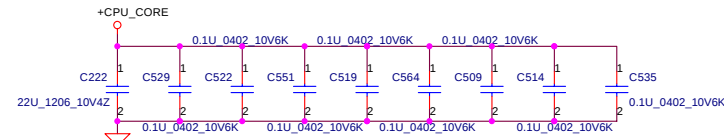
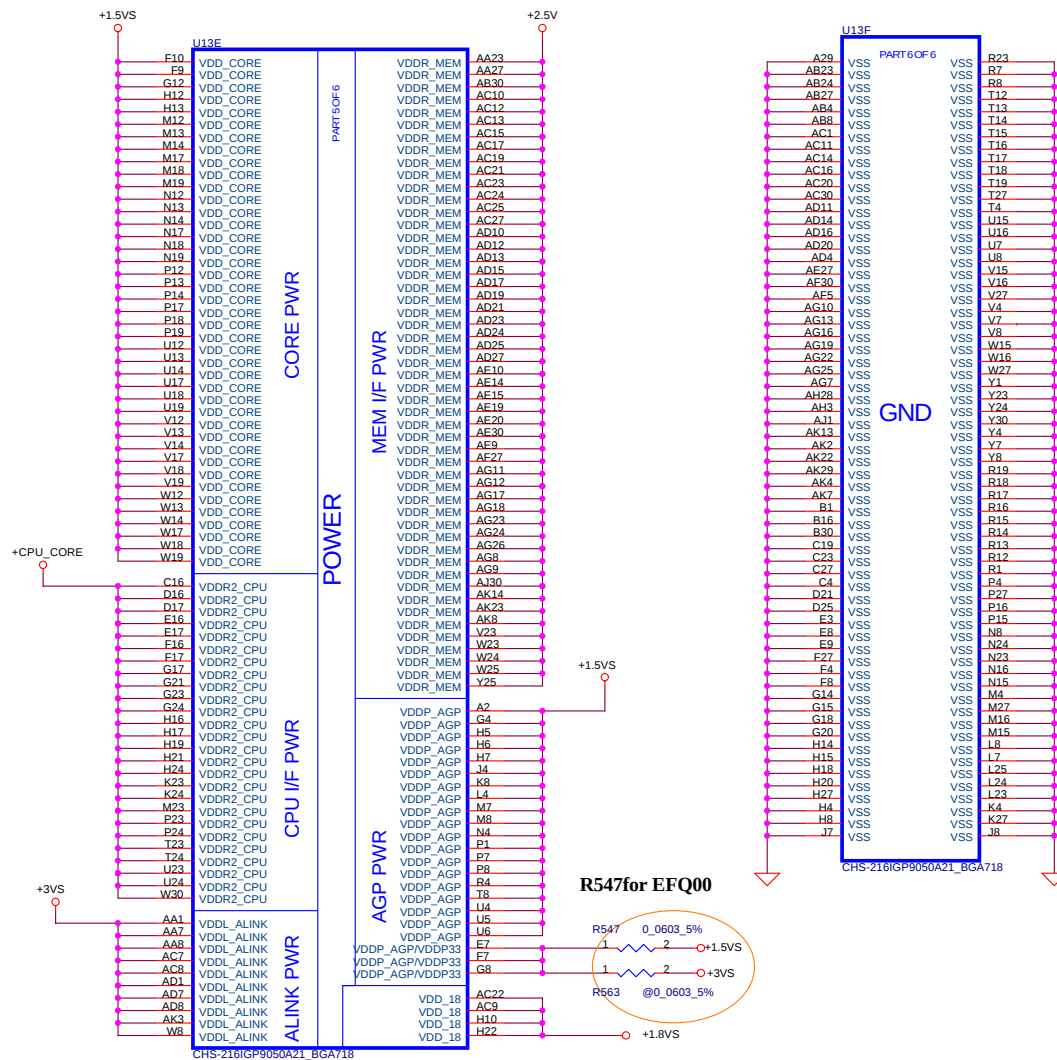


PCI Bus 0 / A-Link I/F
PCI BUS 1 / AGP Bus (GPIO , TMD5 , ZVPort)



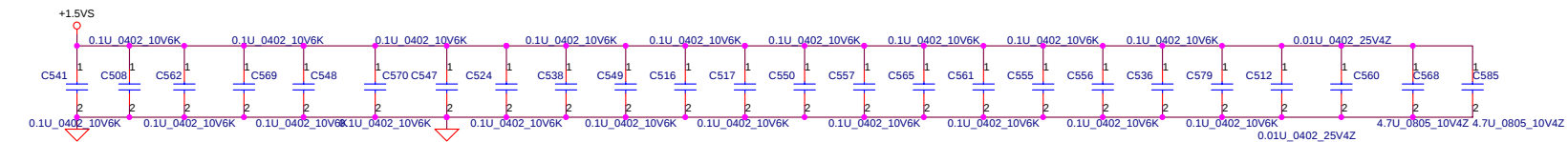
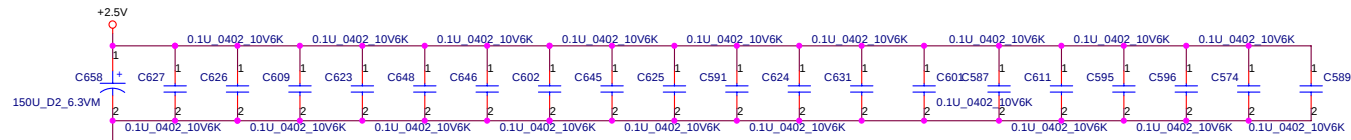
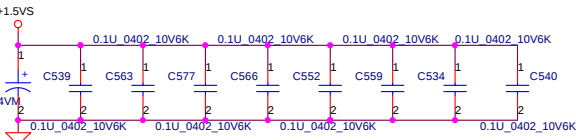
POP For EFQ00
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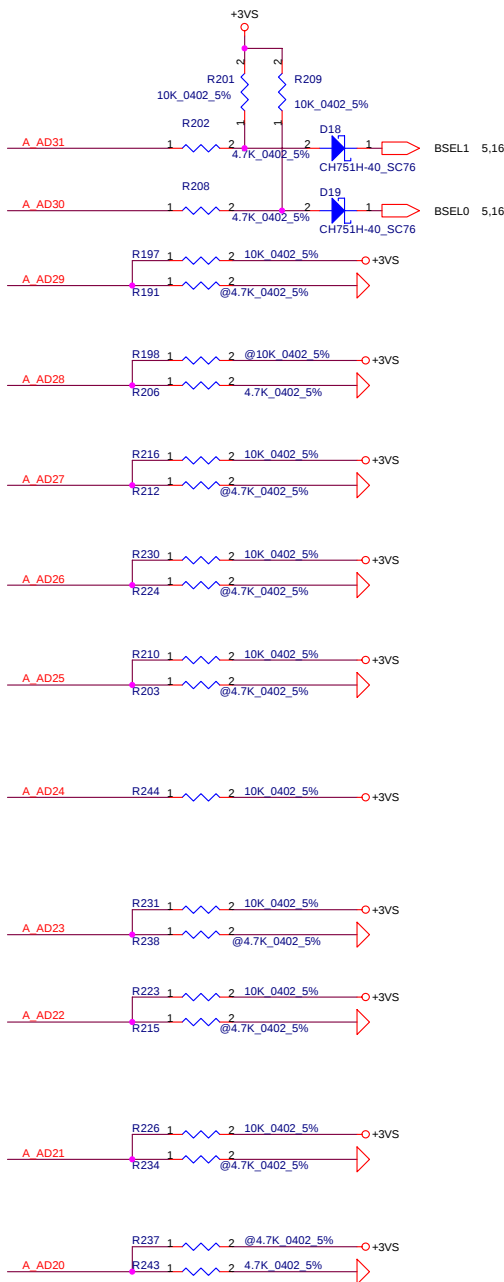
R547for EFQ00

R563 For EEQ00



Compal Electronics, Inc.			
Title			
AT1RC300M-POWER			
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A_AD[31..30] : FSB CLK SPEED
DEFAULT: 01
00: 100 MHZ
01: 133 MHZ
10: 200MHZ
11:166 MHZ

A_AD29: STRAP CONFIGURATION
DEFAULT:1
0:REDUCEDE SET
1: FULL SET

A_AD28: SPREAD SPECTRUM ENABLE
DEFAULT:0
0: DISABLE
1: ENABLE

A_AD27: FrcShortReset#
DEFAULT: 1
0:TEST MODE
1:NORMAL MODE

A_AD26 : ENABLE IOQ
DEFAULT: 1
0: IOQ=1
1: IOQ=12

A_AD25/A_AD17 : CPU VOLTAGE[1..0]
DEFAULT: 10
AD25=1 DESTOP CPU
AD25=0 MOBILE CPU
AD17 -- DON'T CARE

A_AD24 : MOBILE CPU SELECT
DEFAULT: 1
0: BANIAS CPU
1: OTHER CPU

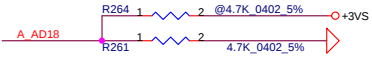
A_AD23 : CLOCK BYPASS DISABLE
DEFAULT: 1
0: TEST MODE
1: NORMAL

A_AD22 : OSC PAD OUTPUT PCICLK
DEFAULT : 1
0: PCICLK OUT
1: OSC CLK OUT

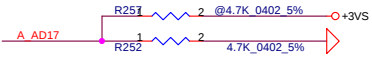
A_AD21 : AUTO_CAL ENABLE
DEFAULT : 1
0: DISABLE
1: ENABLE

A_AD20 : INTERNAL CLK GEN ENABLE
DEFAULT : 0
0: DISABLE
1: ENABLE

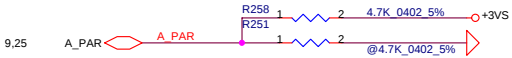
9,25 A_AD[0..31]



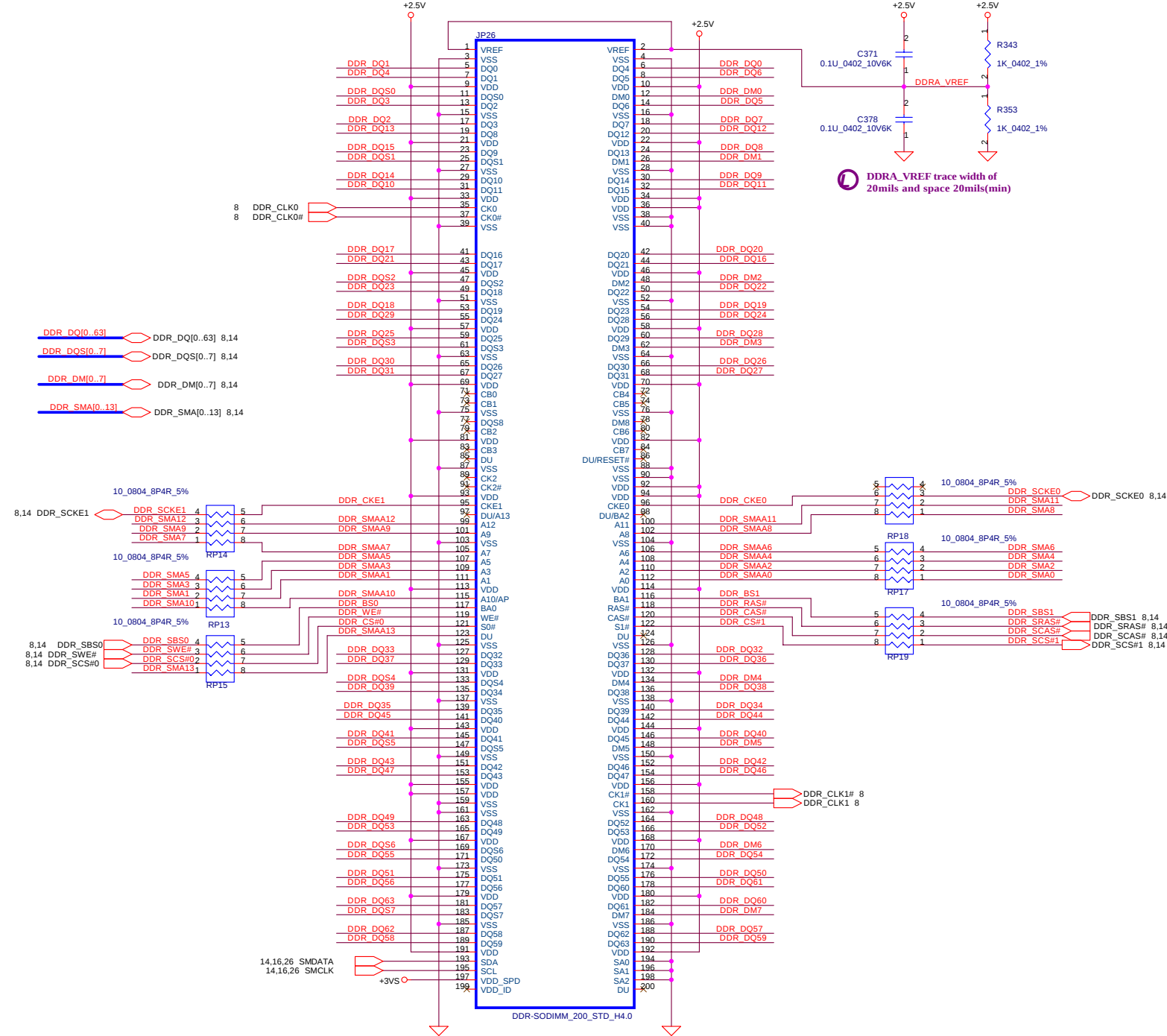
A_AD18 : ENABLE PHASE CALIBRATION
DEFAULT: 0
0: DISABLE
1:ENABLE



A_AD25/A_AD17 : CPU VOLTAGE[1..0]
DEFAULT: 0
00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V



PAR: EXTENDED DEBUG MODE
DEFAULT : 1
0: DEBUG MODE
1: NORMAL



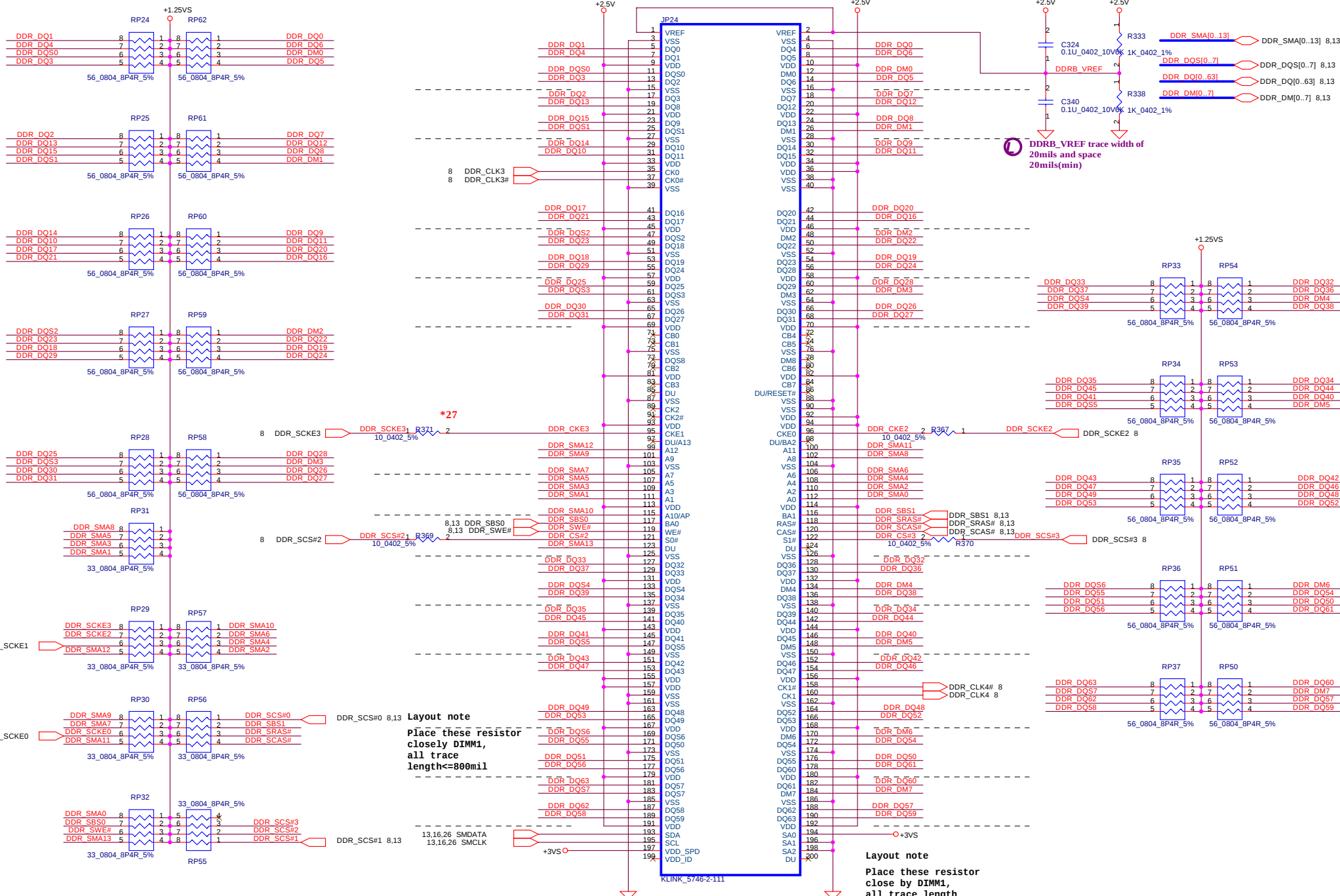
DDR_VREF trace width of 20mils and space 20mils(min)

Layout note

Layout note
Place Add/Command resistors
Close to Pin, max L = 300 mils

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Title			
DDR-SODIMM SLOT0			
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DDR TOPOLOGY 1 FOR SMAA[0, 3, 6:12], SBA[1, 0], SRAS#, SCAS#, SWE#

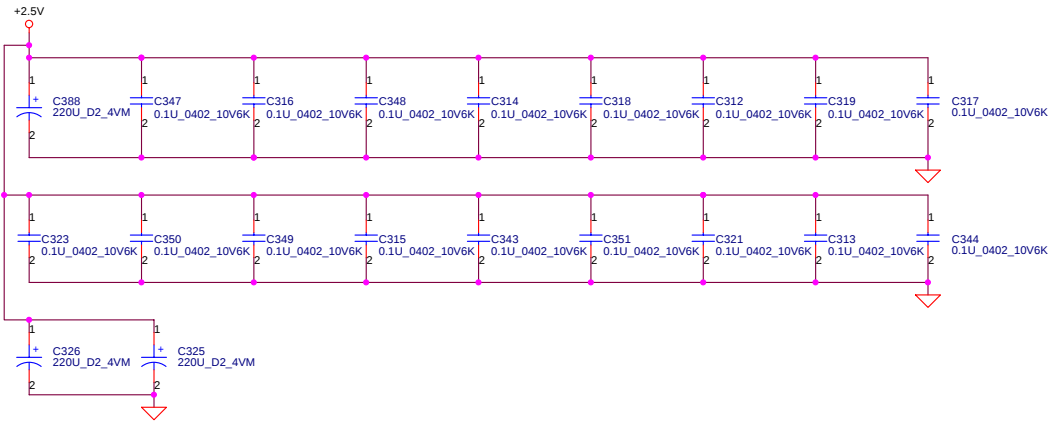
Layout note
Place these resistor
closely DIMM1,
all trace
length<=800mil

Layout note
Place these resistor
close by DIMM1,
all trace length
Max=0.8"

Compal Electronics, Inc.			
Title			
DDR-SODIMM SLOT1			
Size	Document Number		Rev
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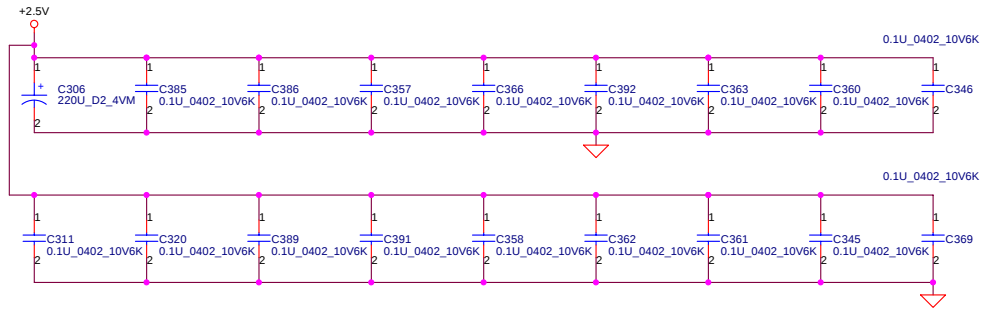
Layout note :
Distribute as close as possible
to DDR-SODIMM0.



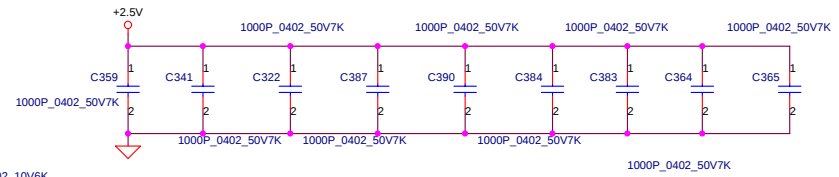
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25VS



Layout note :
Distribute as close as possible
to DDR-SODIMM1.

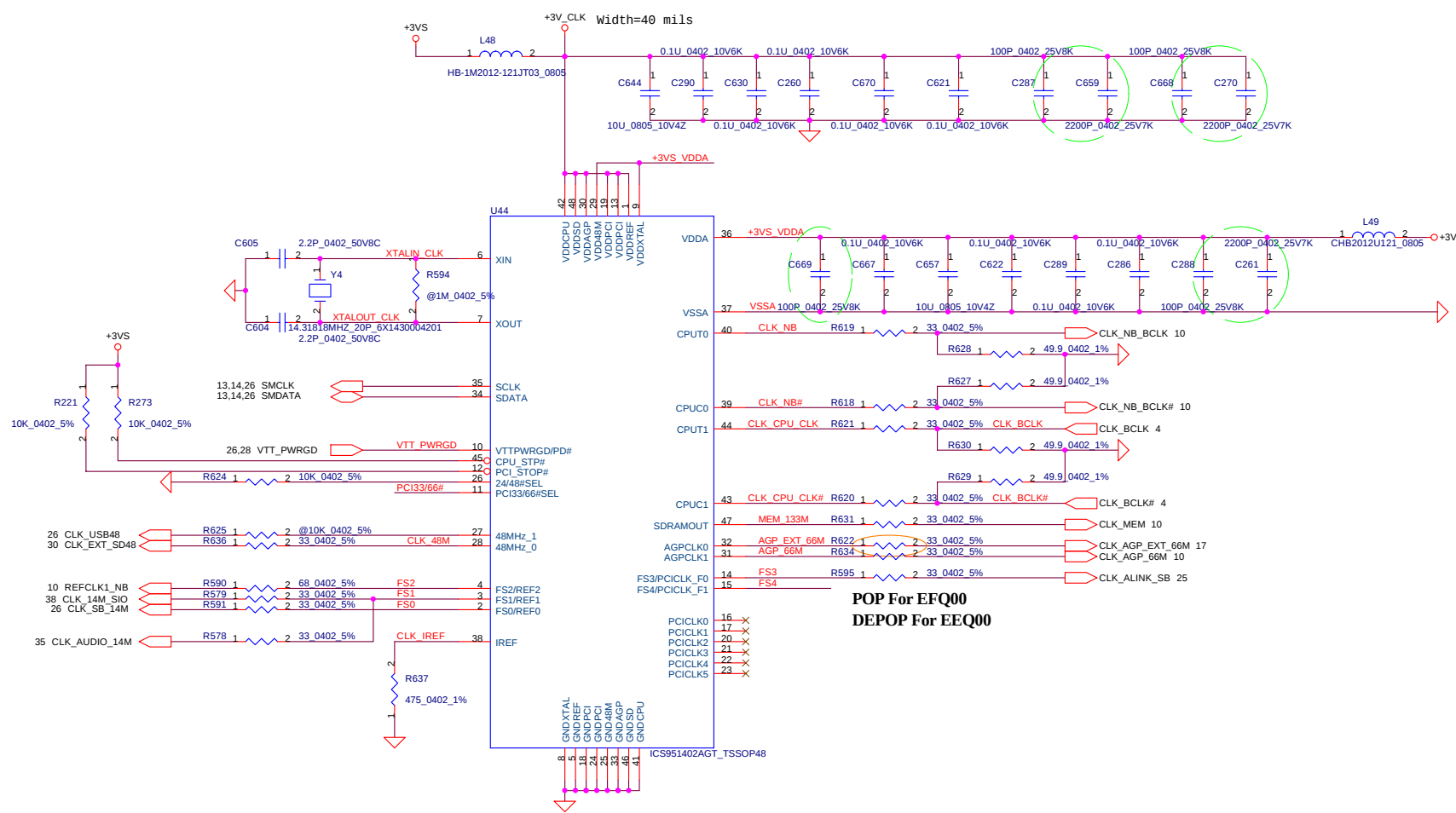


Layout note :
for EMI solution



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Title			
DDR SODIMM Decoupling			
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POP For EFQ00
DEPOP For EEQ00

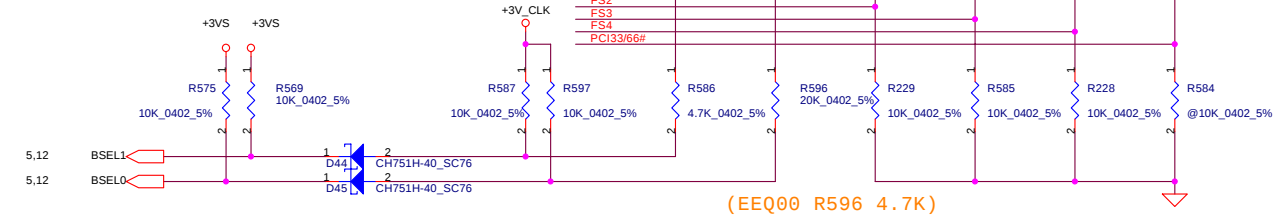
CLOCK FREQUENCY SELECT TABLE

FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled...
0	0	0	1	0	200	200	Spread OFF OR Center spread +/-0.3%
0	0	0	0	1	133	133	
0	0	0	0	0	100	100	

A-LINK FREQ

PC133/66# = HIGH	66MHZ
PC133/66# = LOW	33MHZ

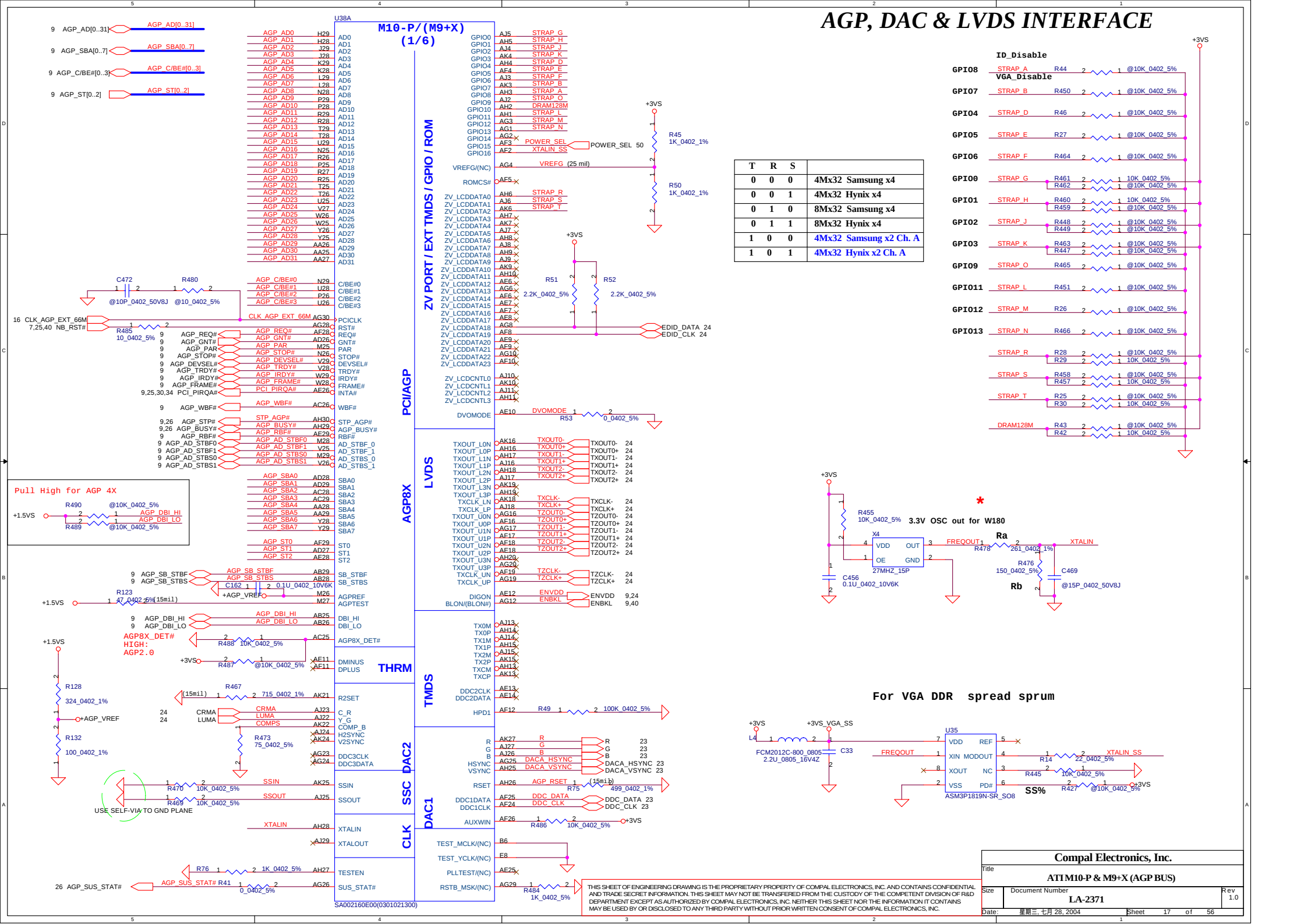
Note: 0 = PULL LOW
1 = PULL HIGH



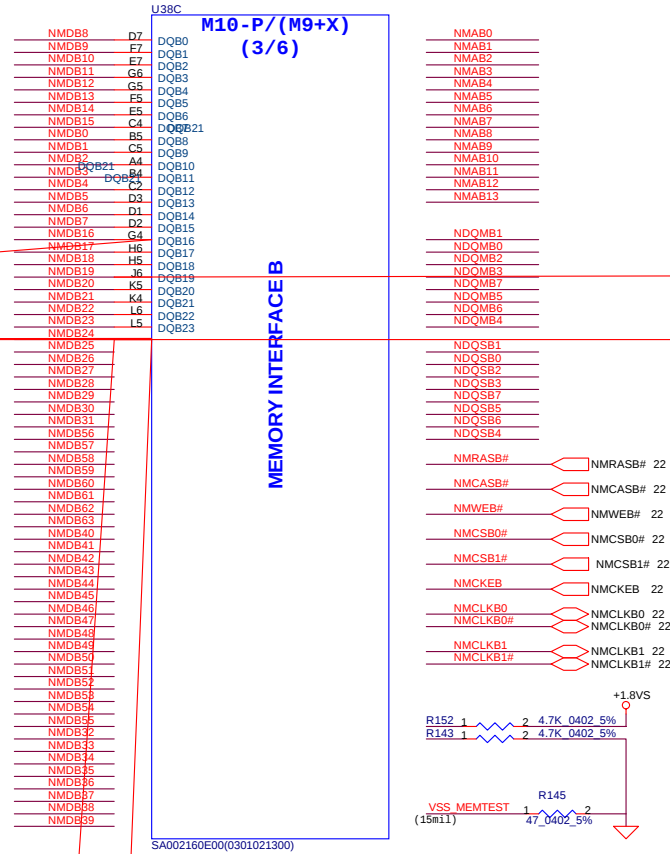
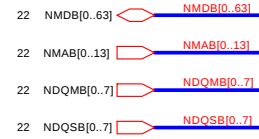
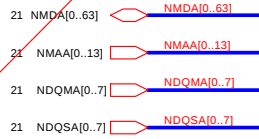
(EEQ00 R596 4.7K)

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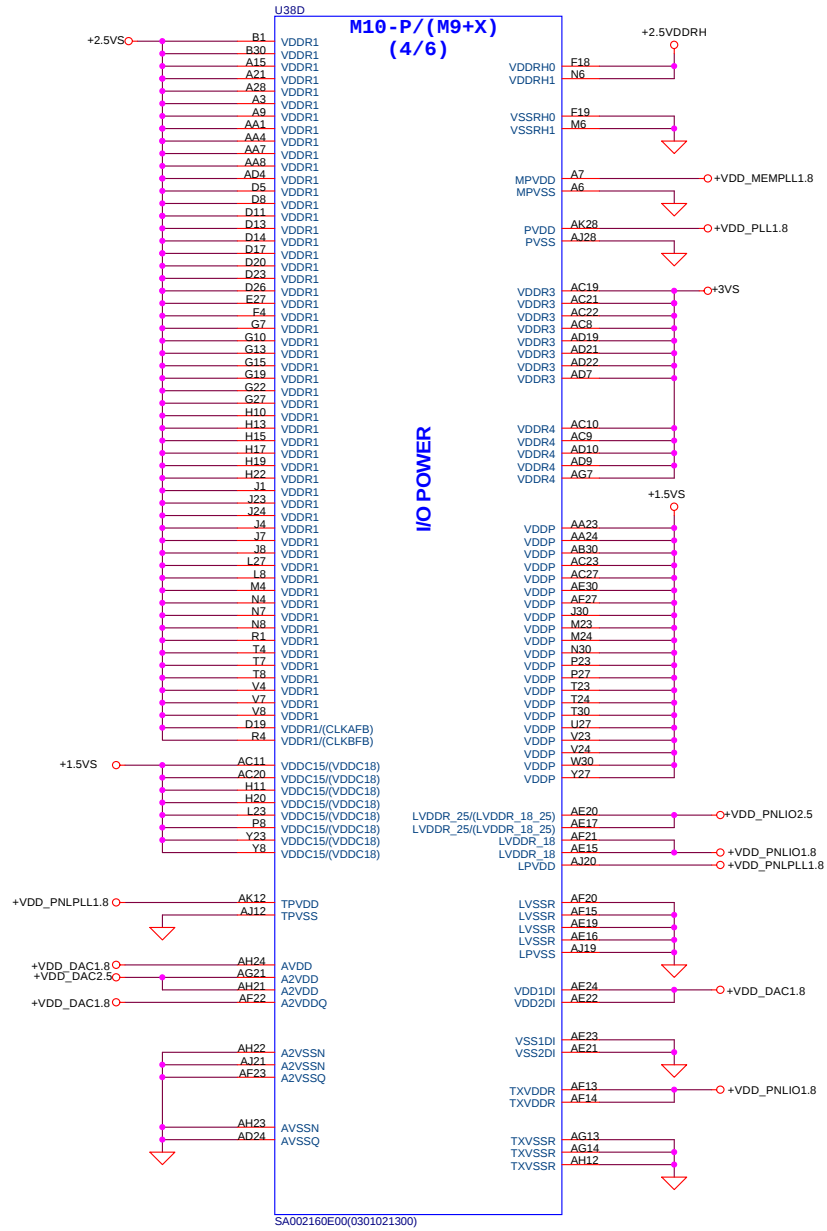
AGP, DAC & LVDS INTERFACE



MEMORY INTERFACE A



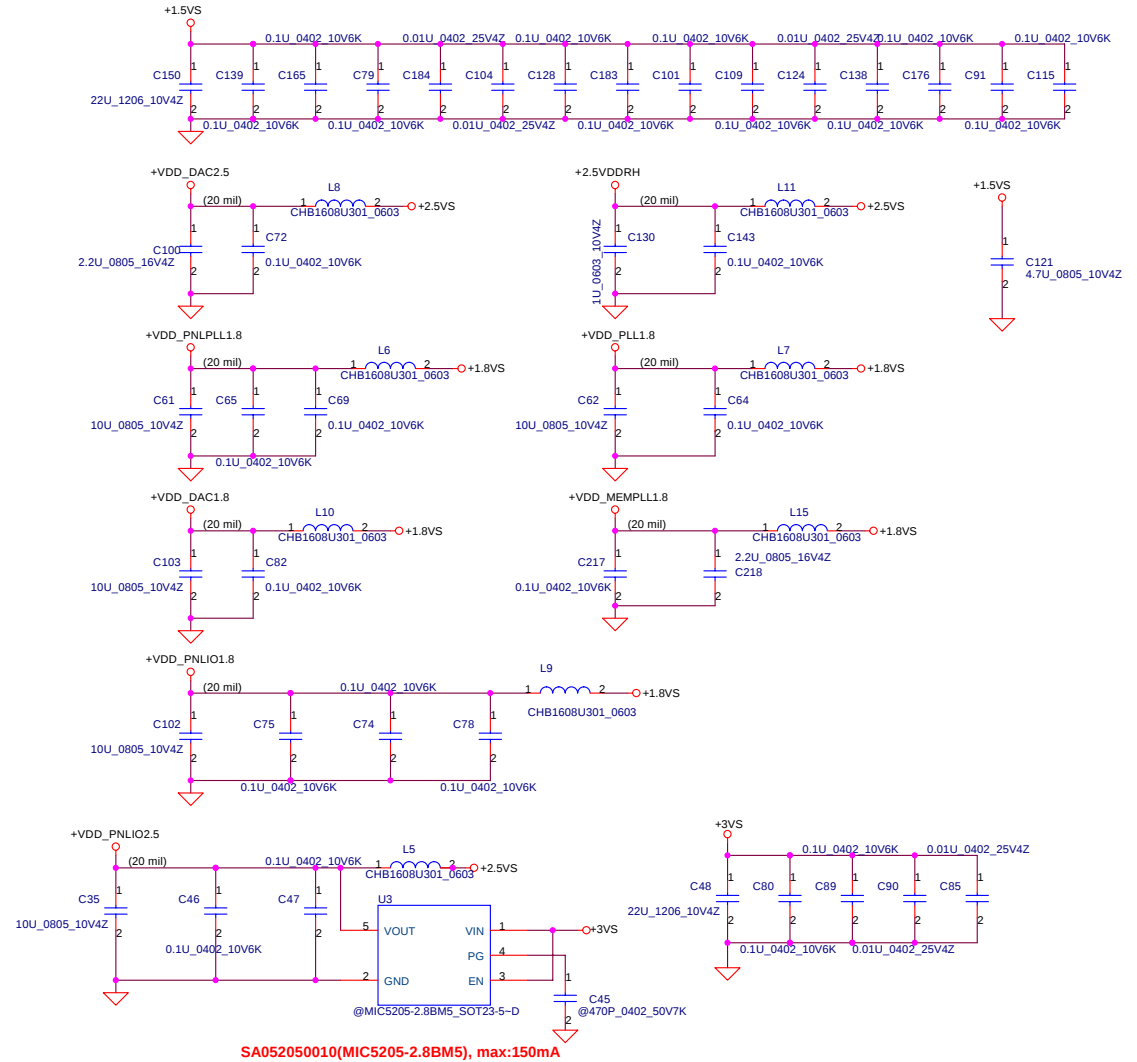
POWER INTERFACE



POWER Sequence

3.3VS --> 2.5VS --> 1.8VS --> +VGA_Core --> +1.5VS

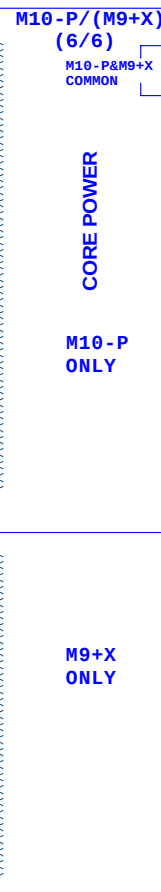
The differ between +2.5VS and +1.8VS should not be greater than 1.2V



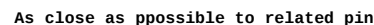
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CORE POWER

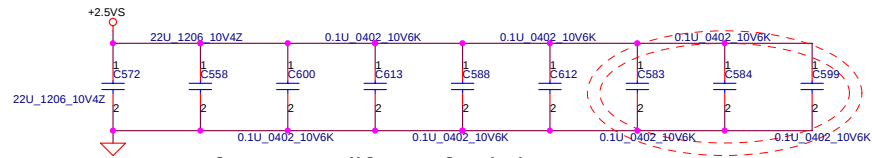


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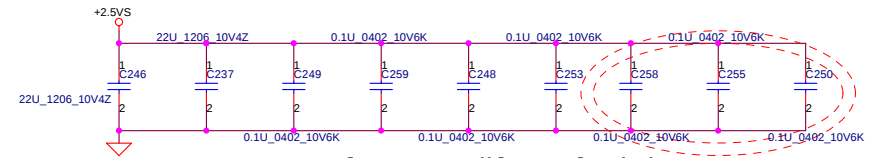


Compal Electronics, Inc.			
Title			
AT11M10-P/M9+X POWER-B			
Size	Document Number		Rev
	LA-2371		1.0
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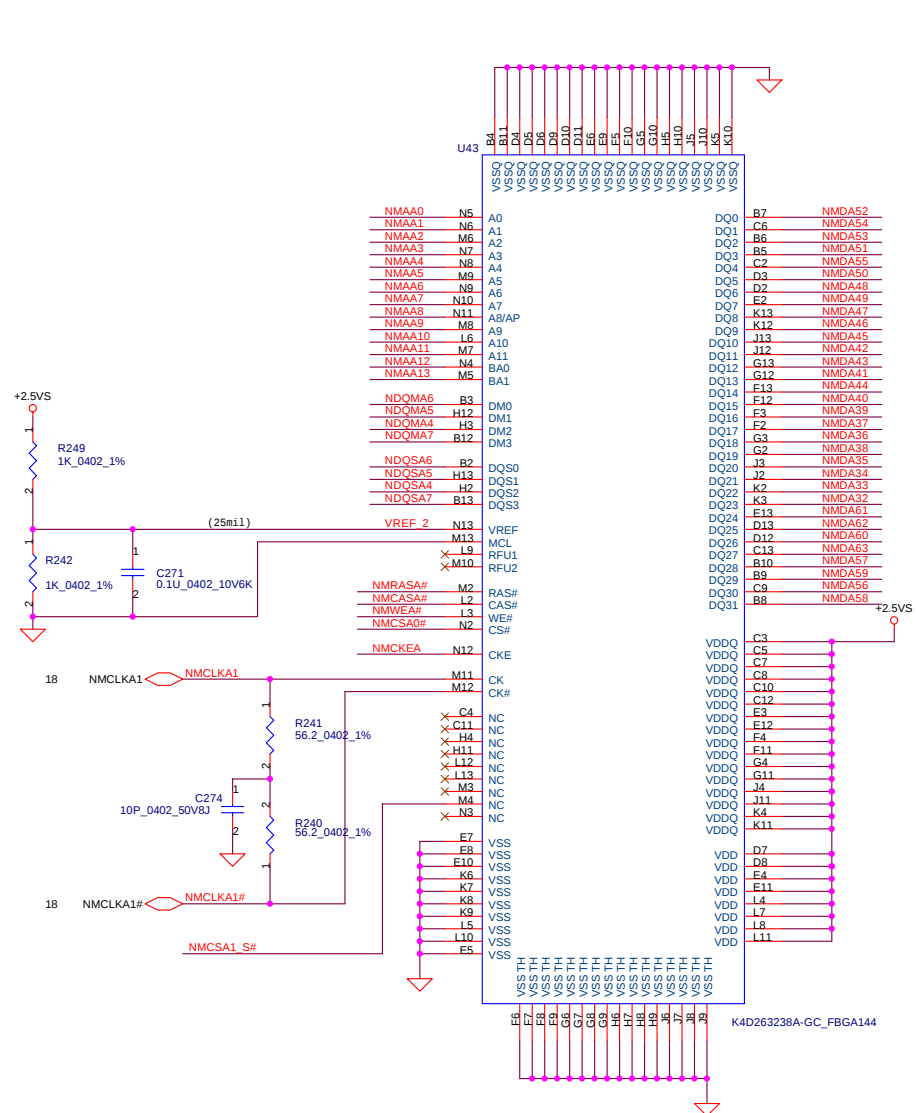
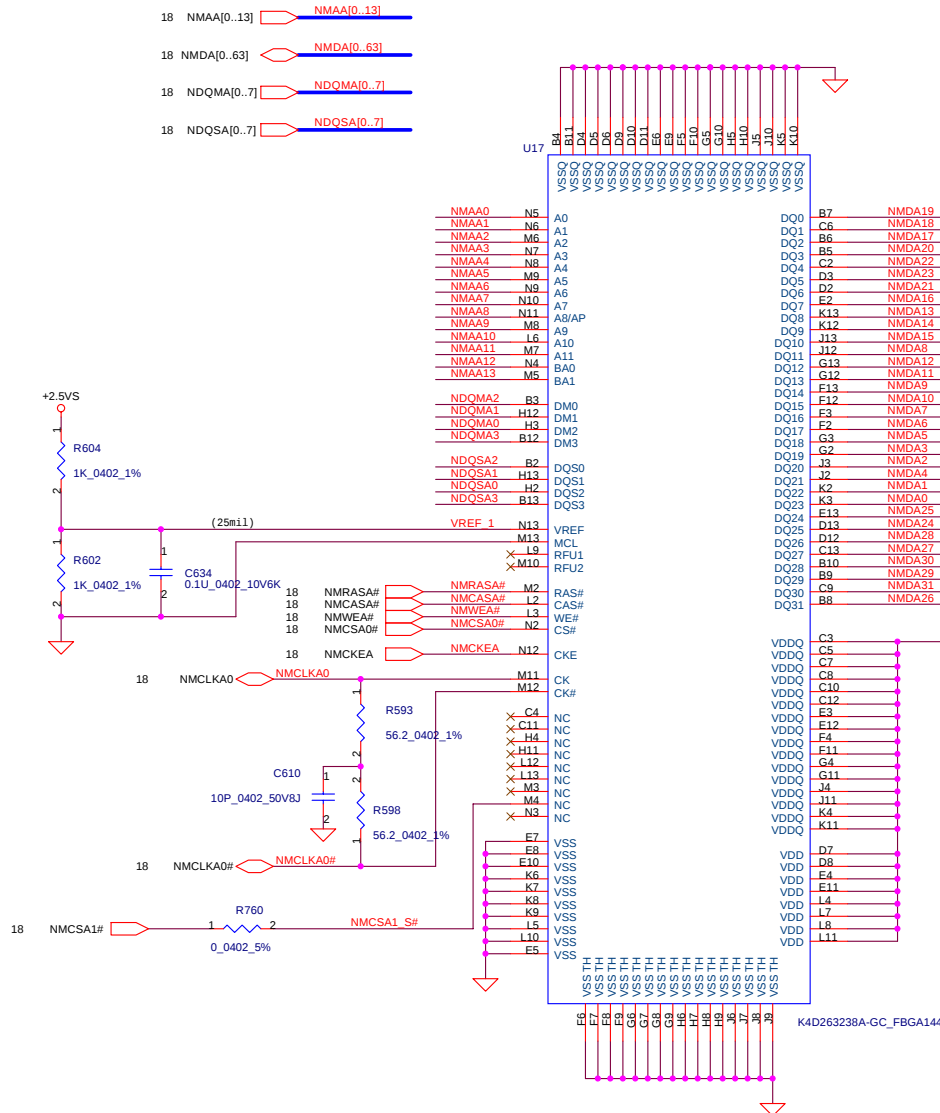
VGA DDR FOR CHANNEL A



As close as ppossible to related pin

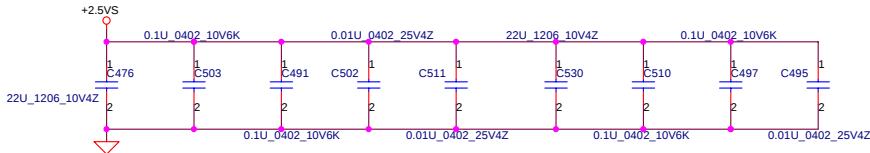


As close as ppossible to related pin



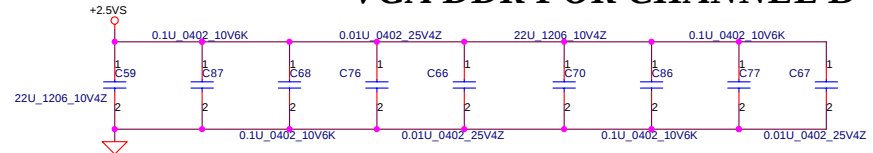
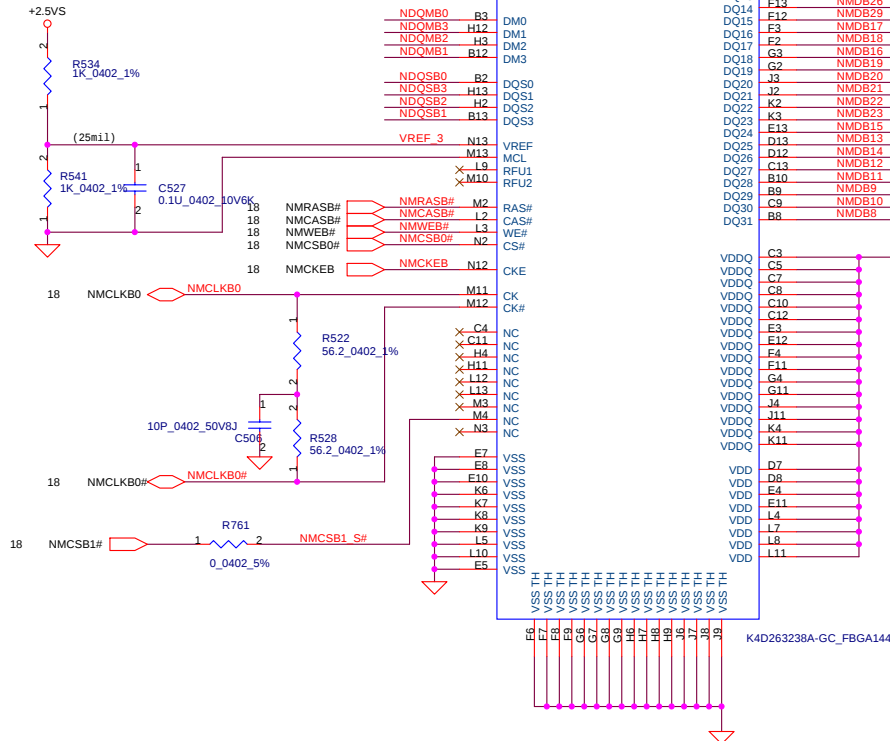
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VGA DDR FOR CHANNEL B



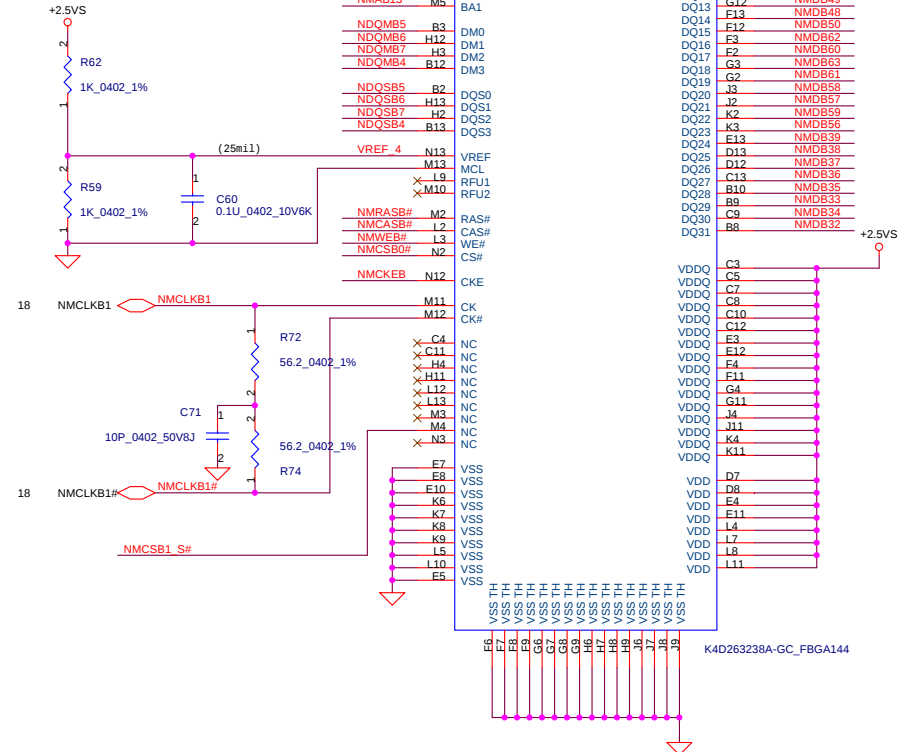
As close as possible to related pin

18 NMAB[0..13] NMAB[0..13]
18 NMDB[0..63] NMDB[0..63]
18 NDQMB[0..7] NDQMB[0..7]
18 NDQSB[0..7] NDQSB[0..7]



As close as possible to related pin

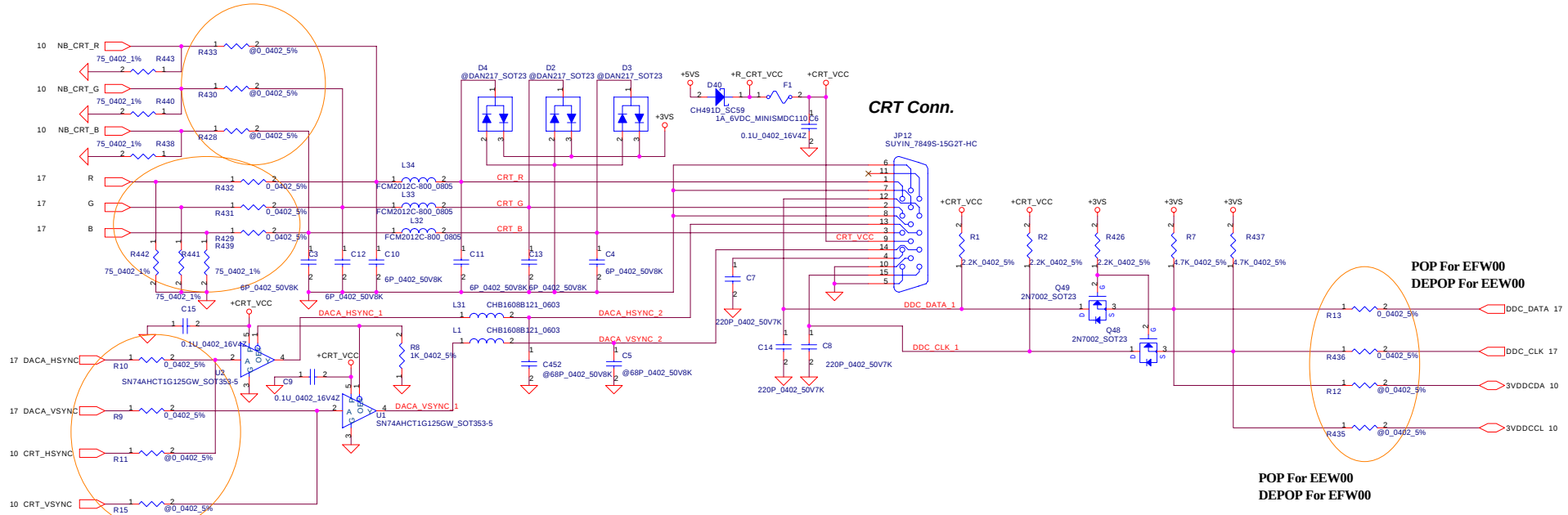
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18 NMDB[0..63] NMDB[0..63]
18 NDQMB[0..7] NDQMB[0..7]
18 NDQSB[0..7] NDQSB[0..7]



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VGA DDR FOR CHANNEL B			
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POP For EFW00
DEPOP For EEW00



CRT Conn.

POP For EFW00
DEPOP For EEW00

POP For EEW00
DEPOP For EFW00

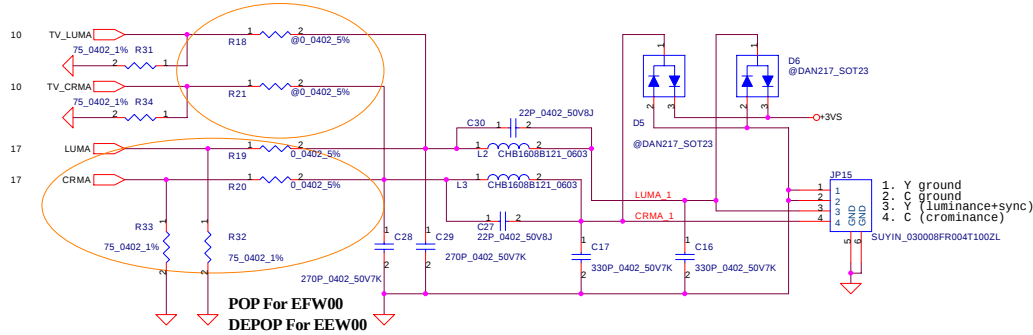
POP For EFW00
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Compal Electronics, Inc.			
Title			
CRT Connector			
Size	Document Number		Rev
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Date:	日期	2004.07.28	Sheet 23 of 56

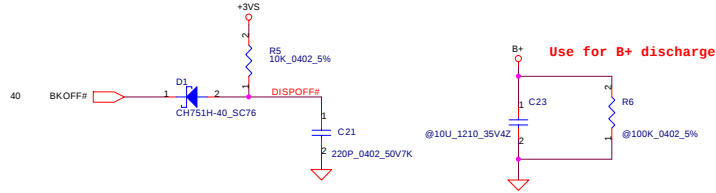
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POP For EEQ00
DEPOP For EFQ00

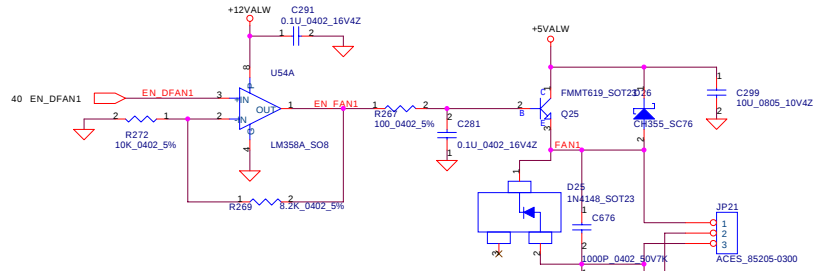
TV-OUT Conn.



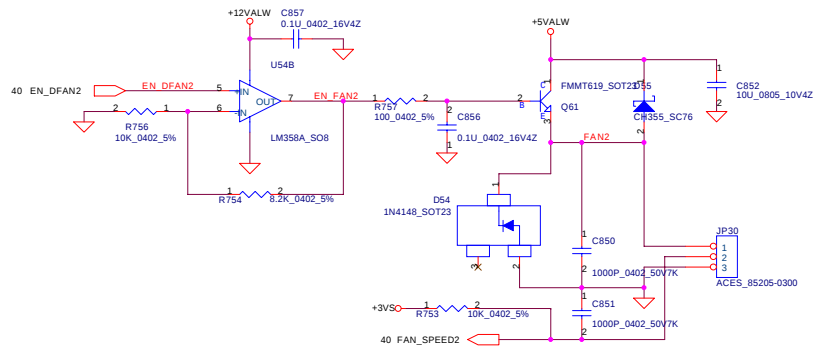
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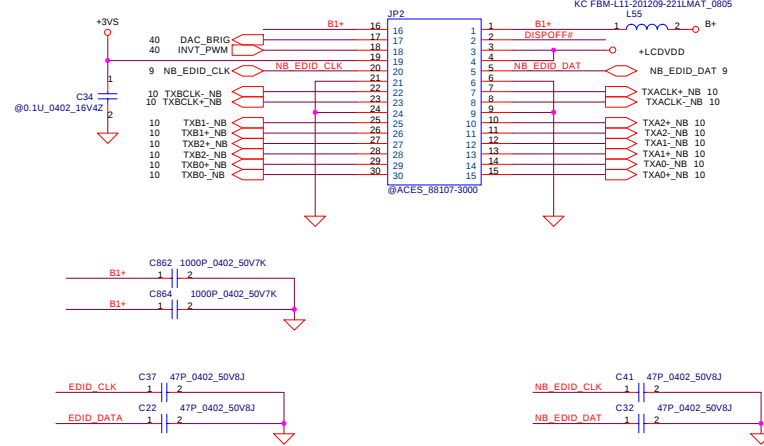
FAN CONN. 1



FAN CONN. 2

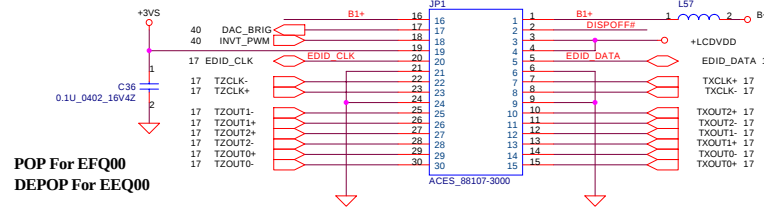


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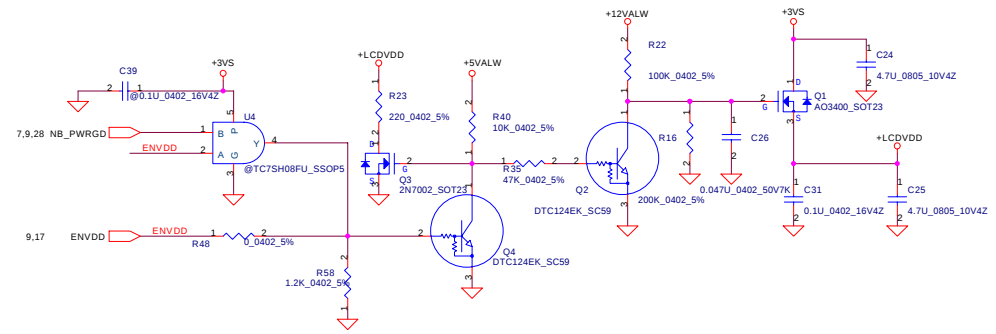


POP For EEQ00
DEPOP For EFQ00

Width: 40mils



POP For EFQ00
DEPOP For EEQ00

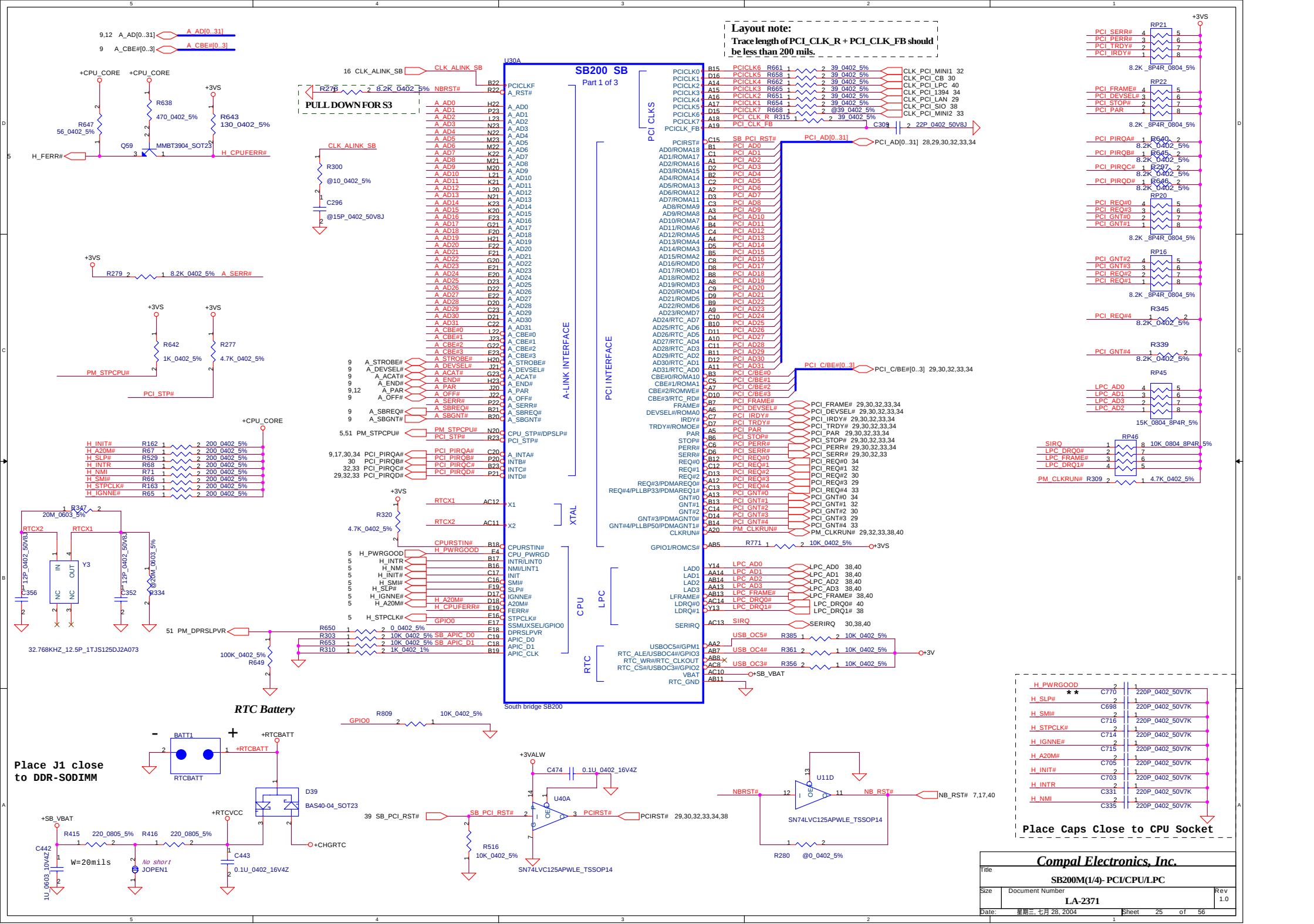


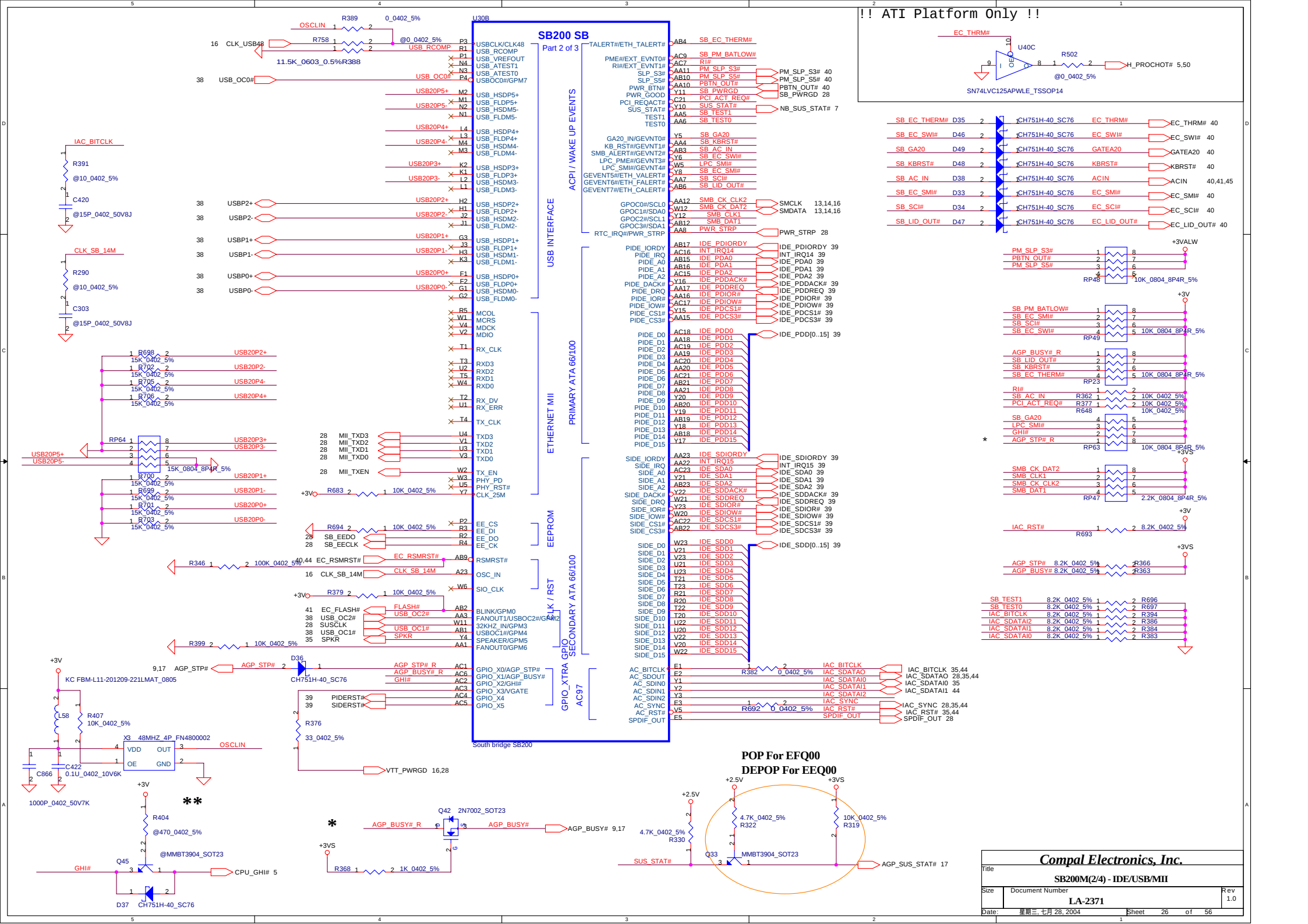
Compal Electronics, Inc.

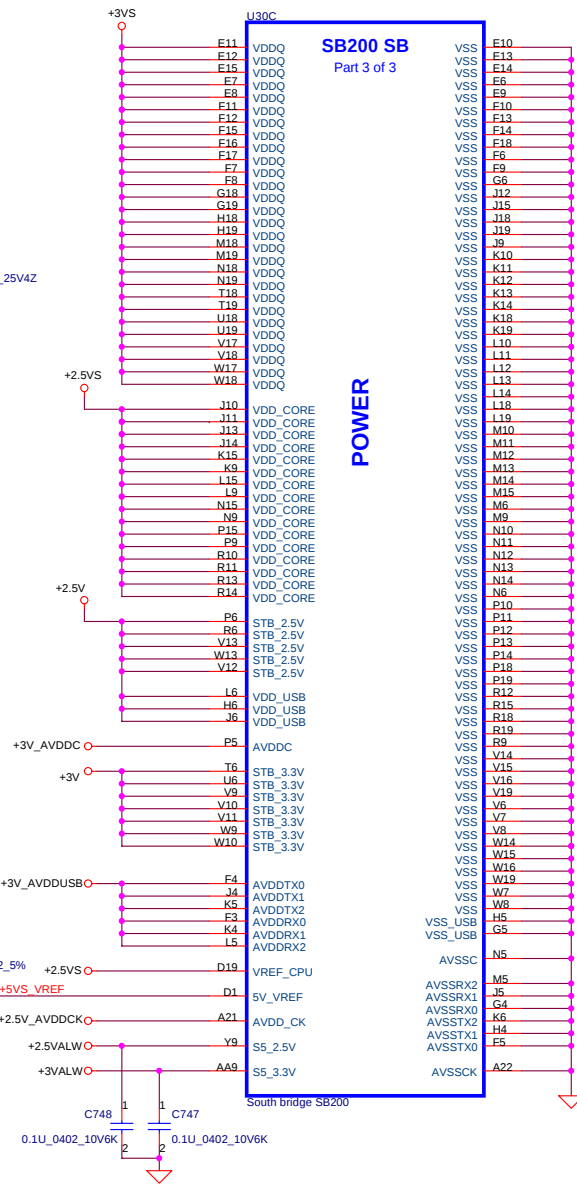
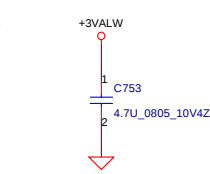
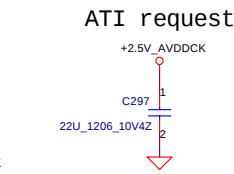
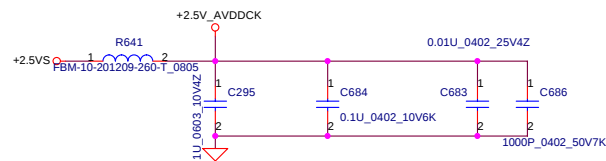
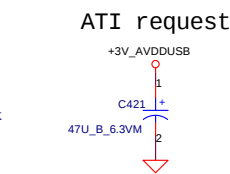
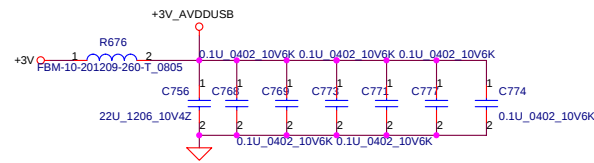
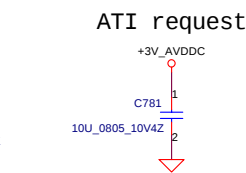
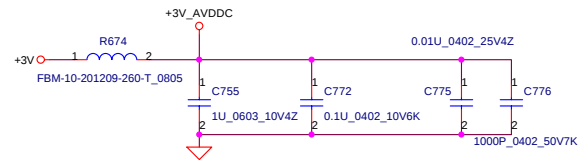
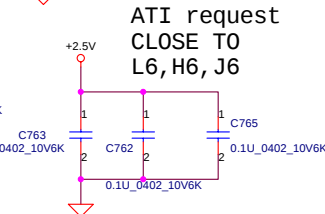
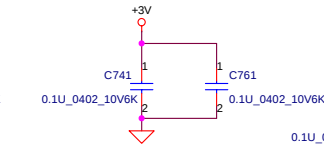
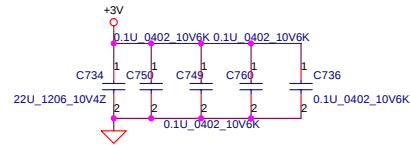
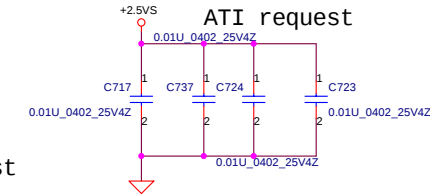
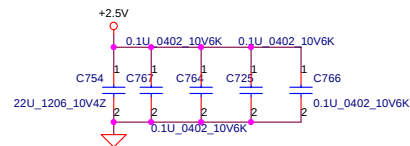
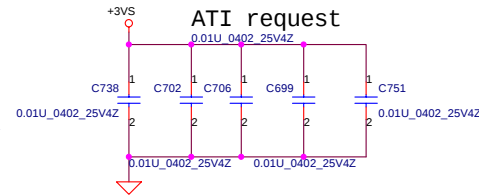
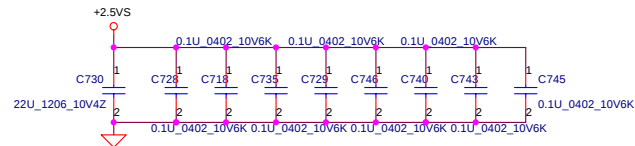
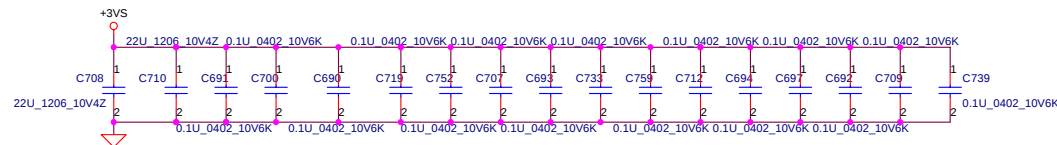
CRT,TV-OUT & LVDS Connector

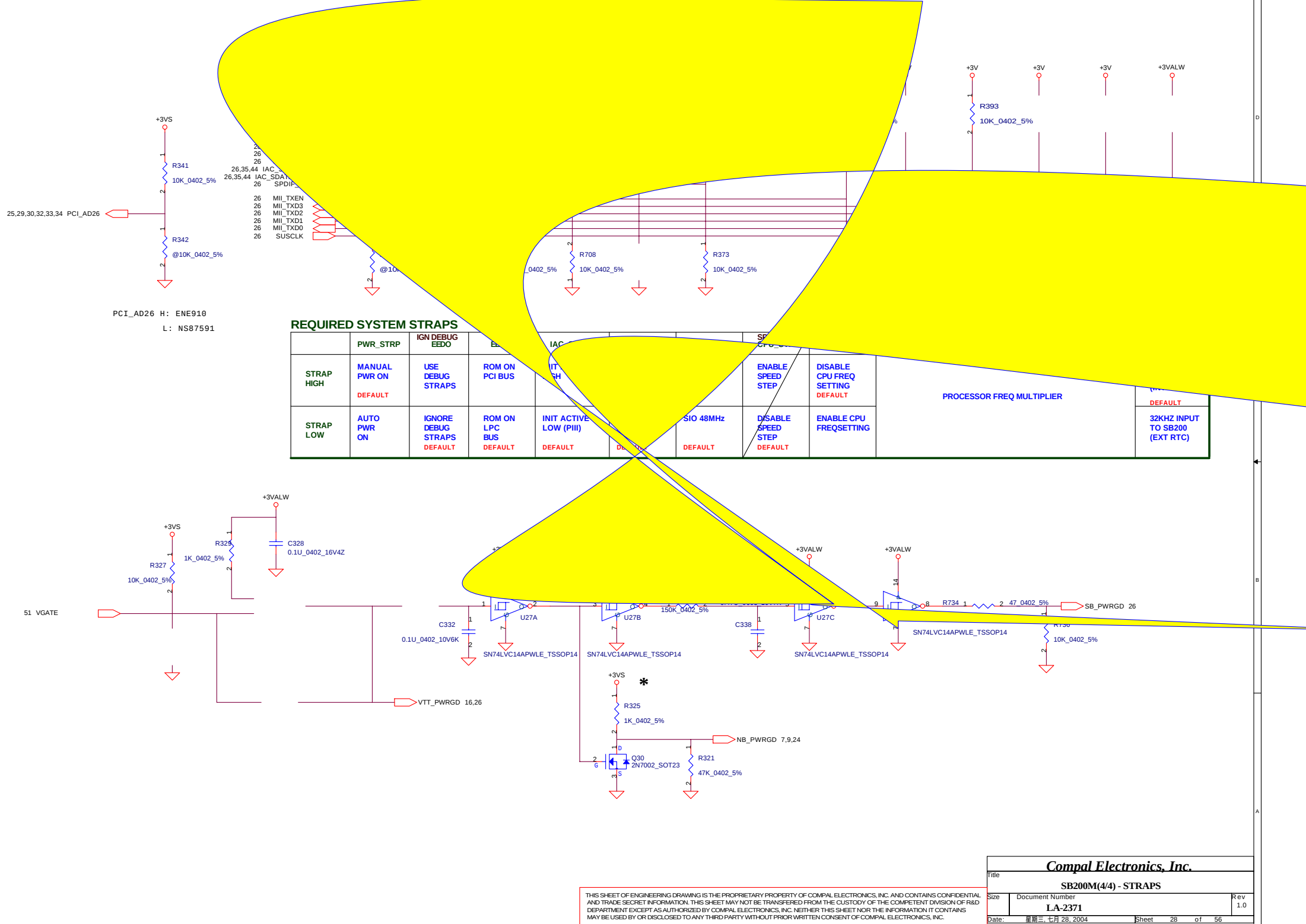
Size C Document Number LA-2371 Rev 1.0
Date: 七月 26, 2004 Sheet 24 of 56

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REQUIRED SYSTEM STRAPS

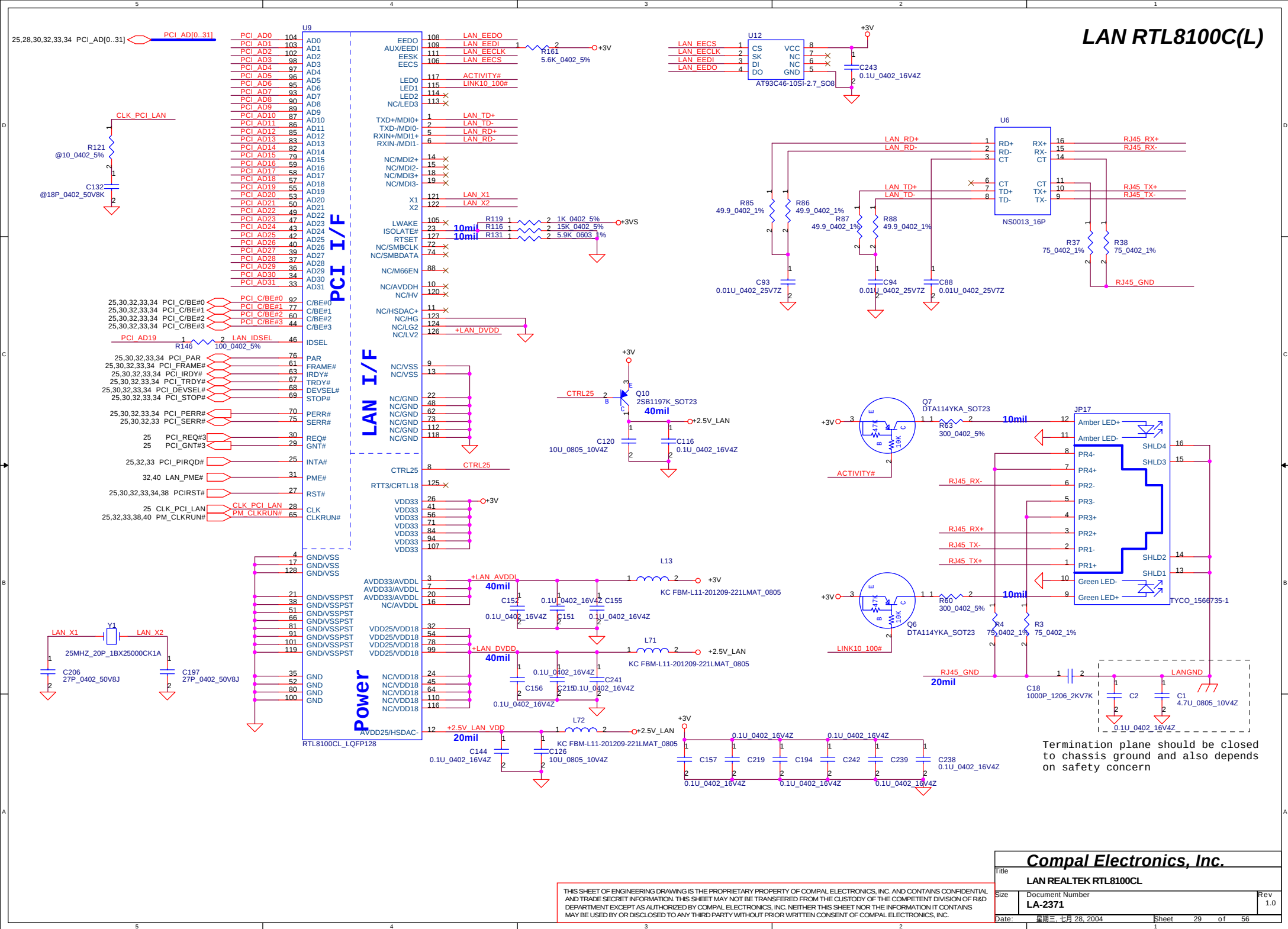
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STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS DEFAULT	INIT ACTIVE LOW (PIII) DEFAULT	SIO 48MHz DEFAULT	ENABLE SPEED STEP DEFAULT	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER DEFAULT	32KHZ INPUT TO SB200 (EXT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (PIII) DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP DEFAULT	ENABLE CPU FREQ SETTING	PROCESSOR FREQ MULTIPLIER DEFAULT	32KHZ INPUT TO SB200 (EXT RTC) DEFAULT

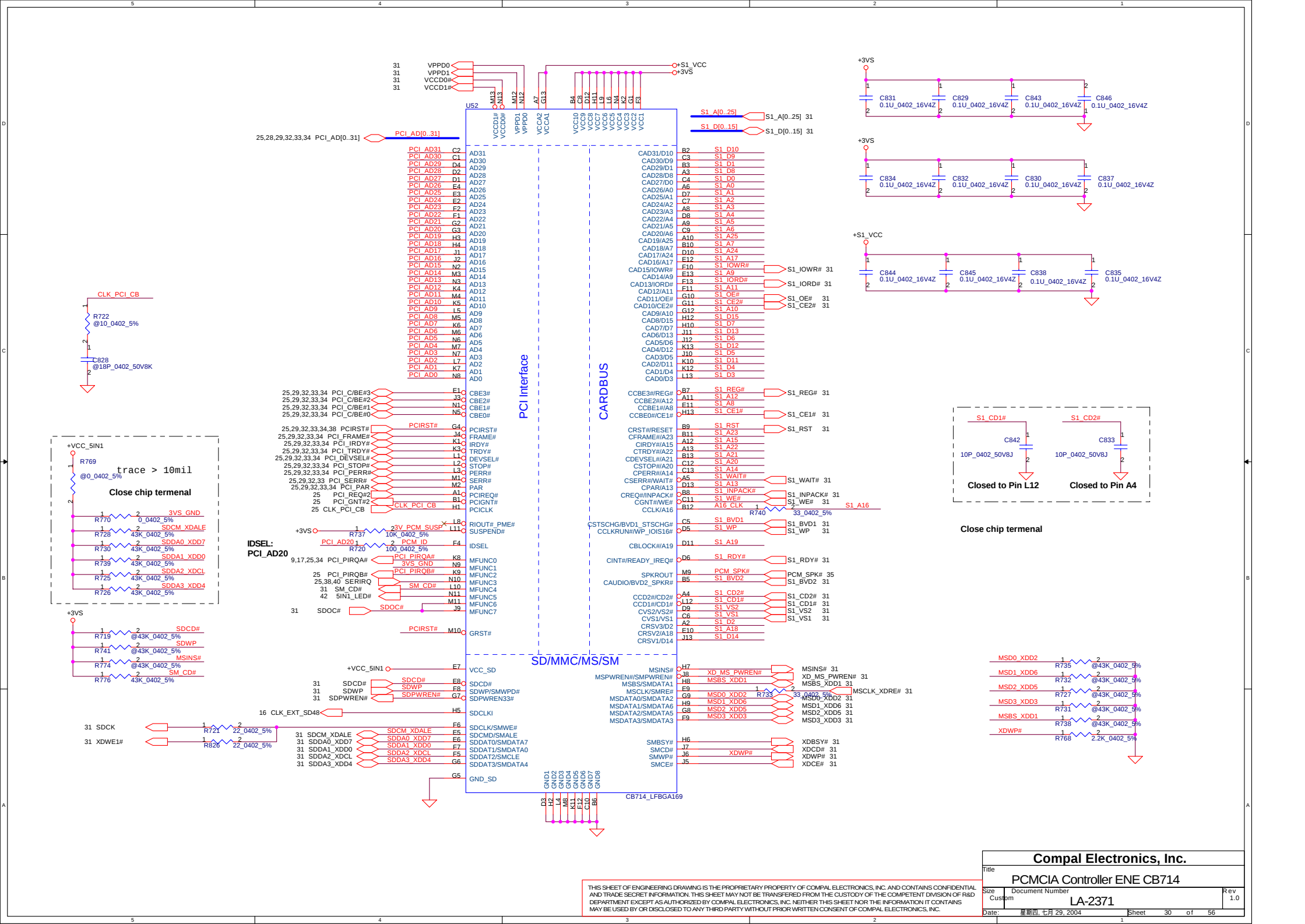
Compal Electronics, Inc.

SB200M(4/4) - STRAPS

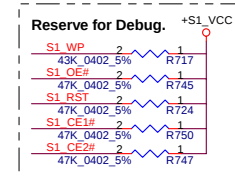
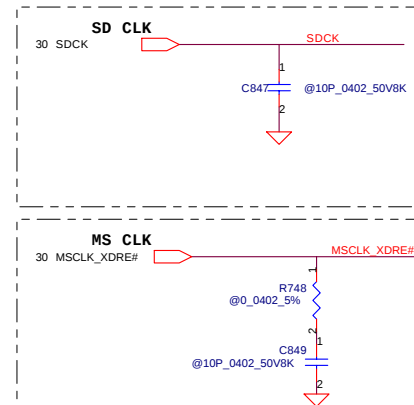
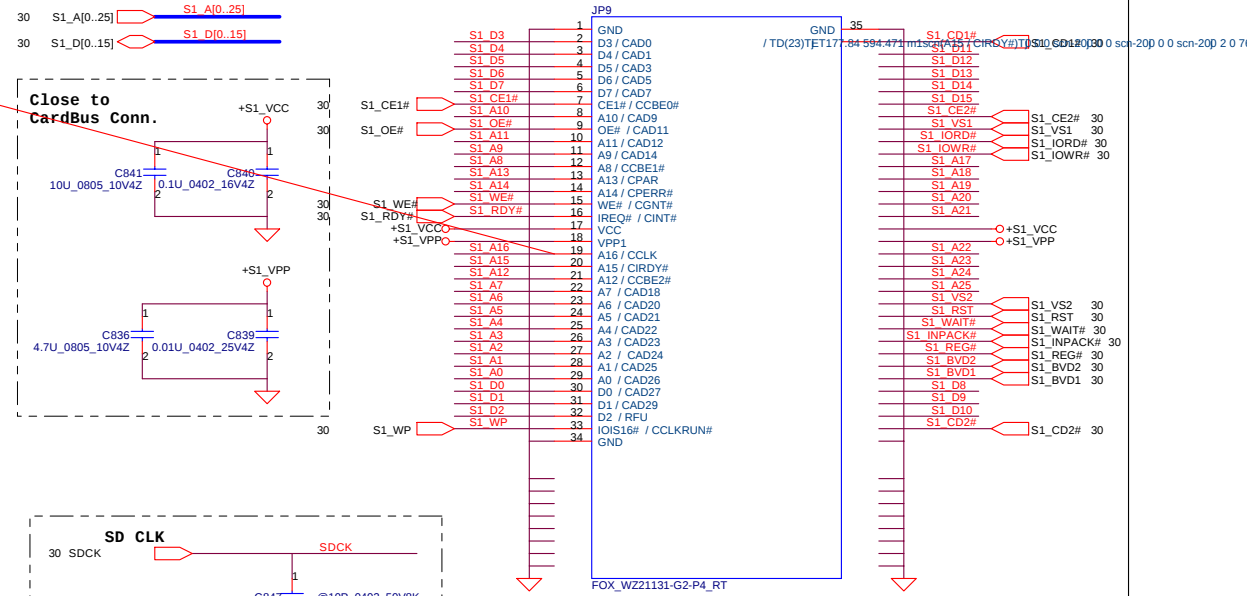
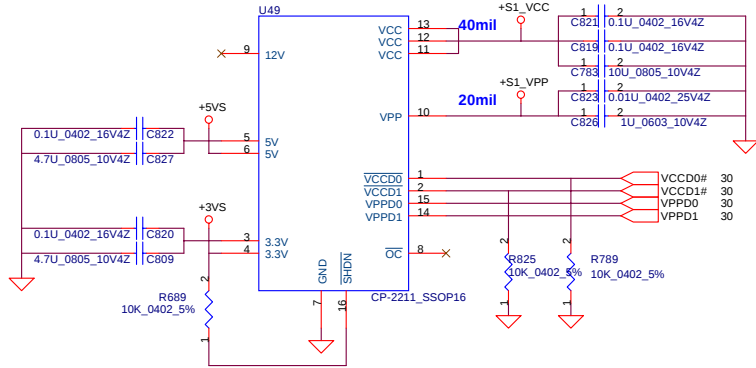
Size	Document Number	Rev
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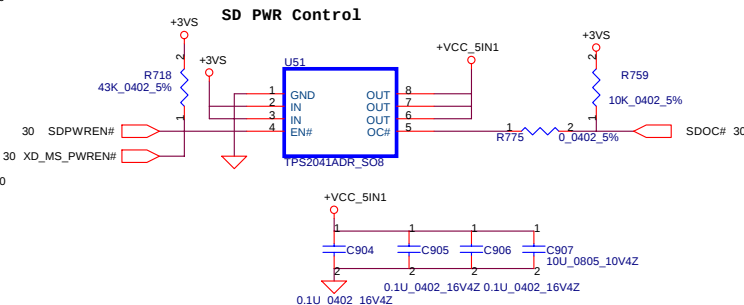
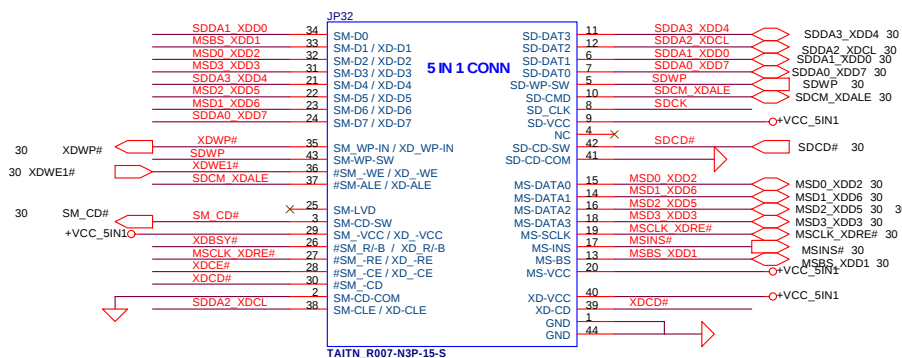
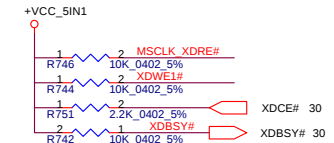


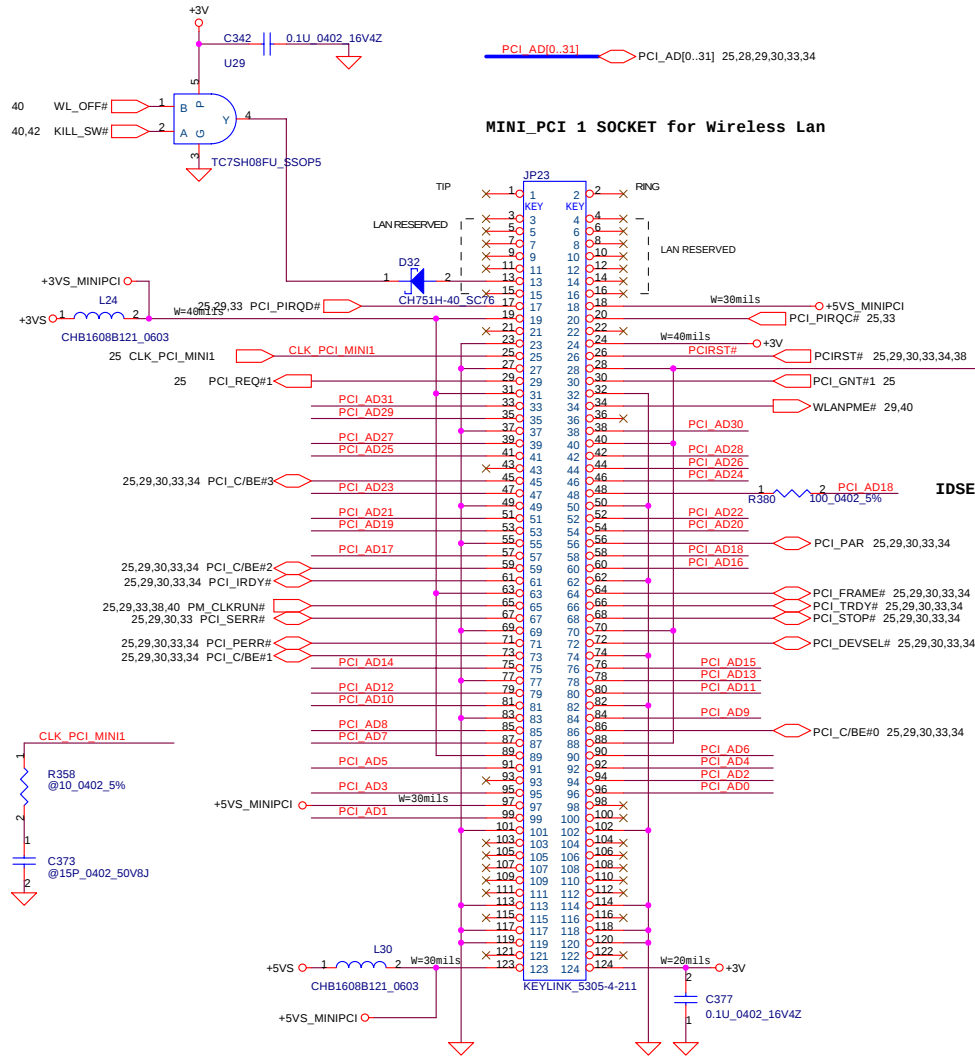


~~PCMCIA Power Controller~~

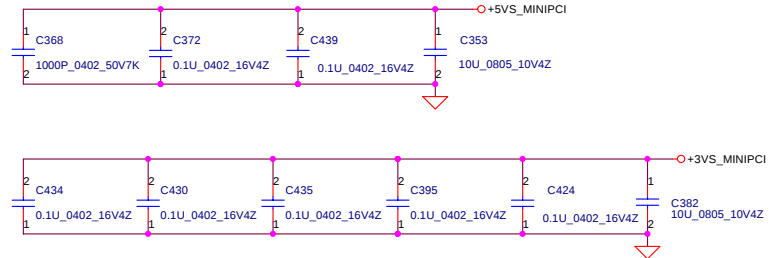
CardBus Socket

xD PU and PD. Close to Socket





IDSEL : PCI_AD18



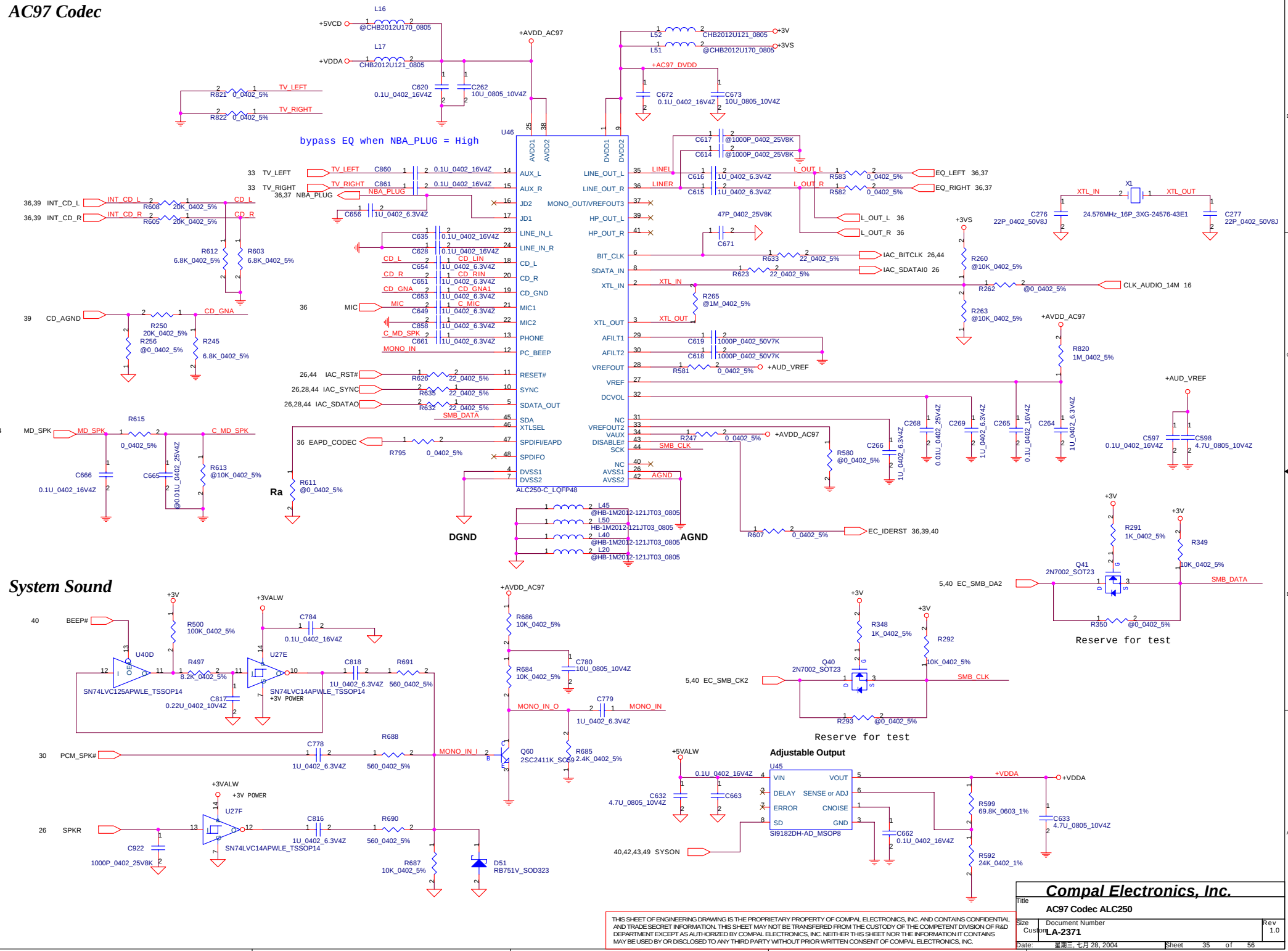
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Title				
MINI_PCI				
Size	Document Number			Rev
Custom	LA-2371			1.0
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AC97 Codec

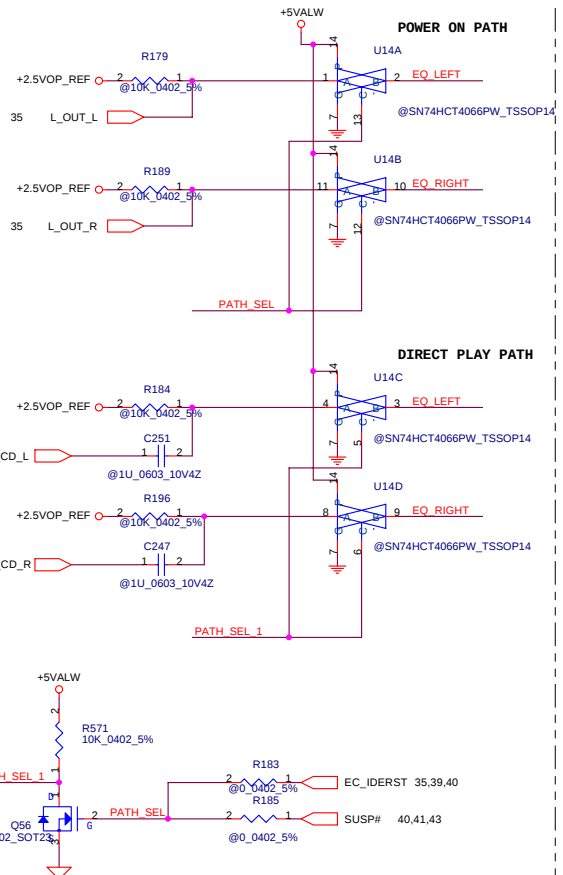
System Sound



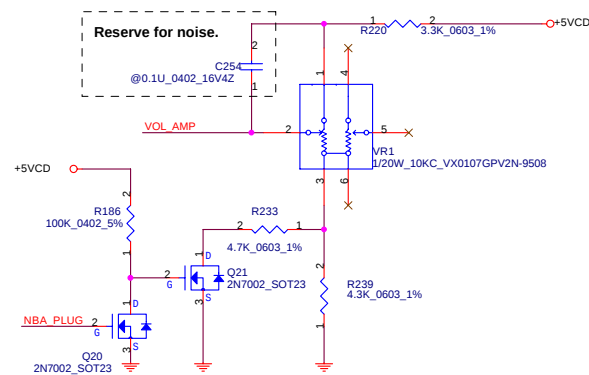
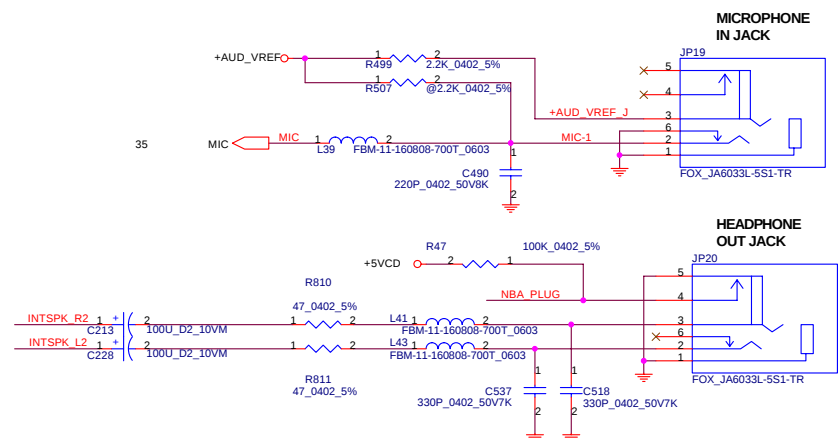
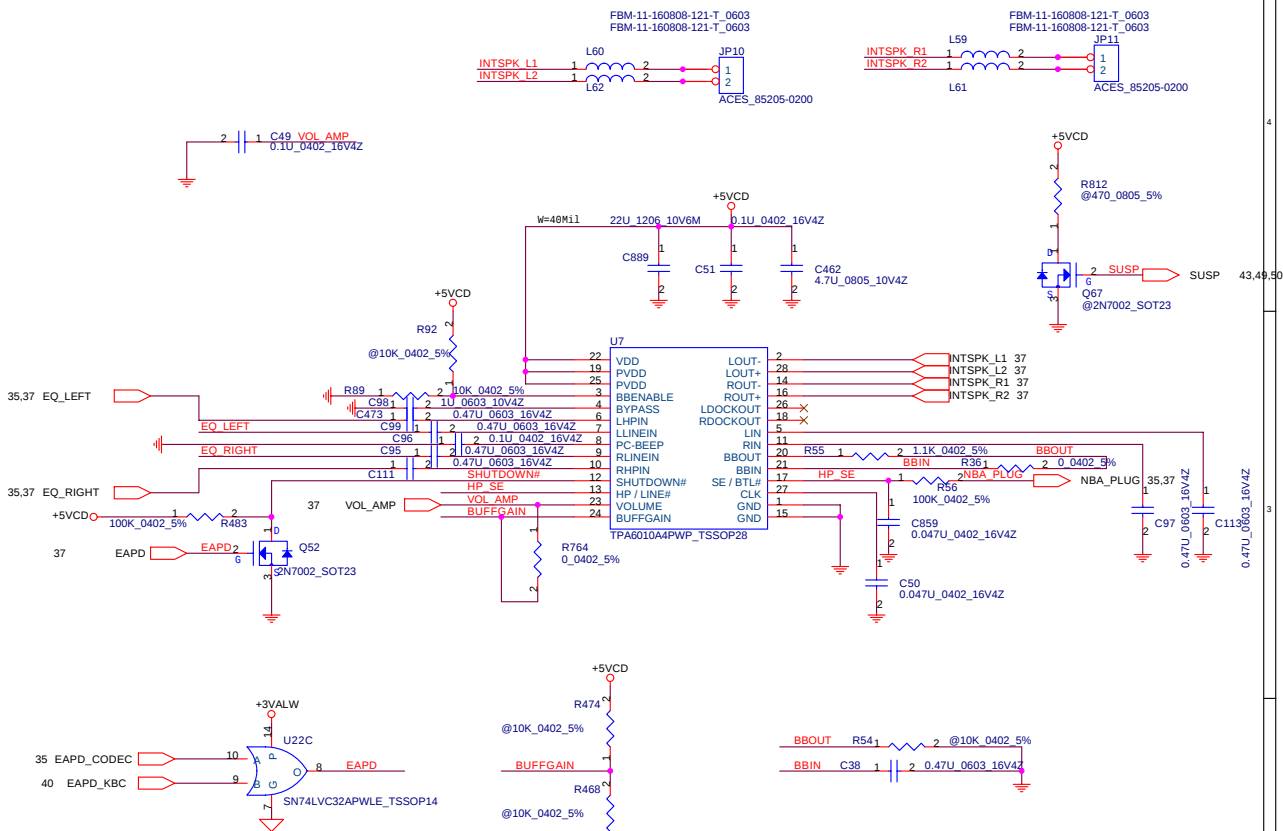
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AC97 Codec ALC250			
Title	Size	Document Number	Rev
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**Direct CD
CTL**



Audio AMP

VR - C-Type

R220	3.3K	Bias (Gain)	SPK 22dB
R233	4.7K		
R239	4.3K		HP -4dB

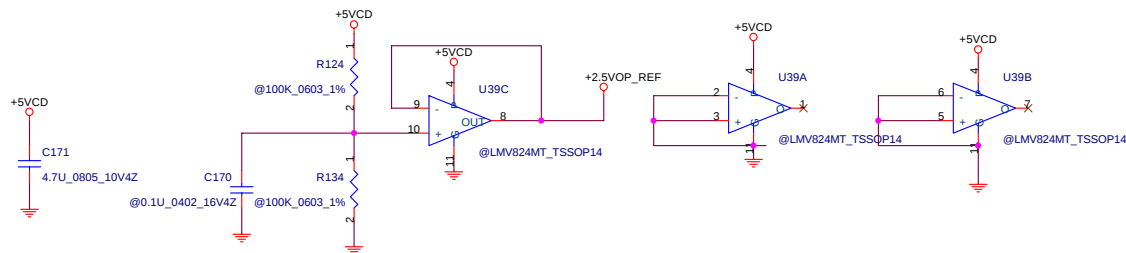
Compal Electronics, Inc.

Audio AMP & JACK

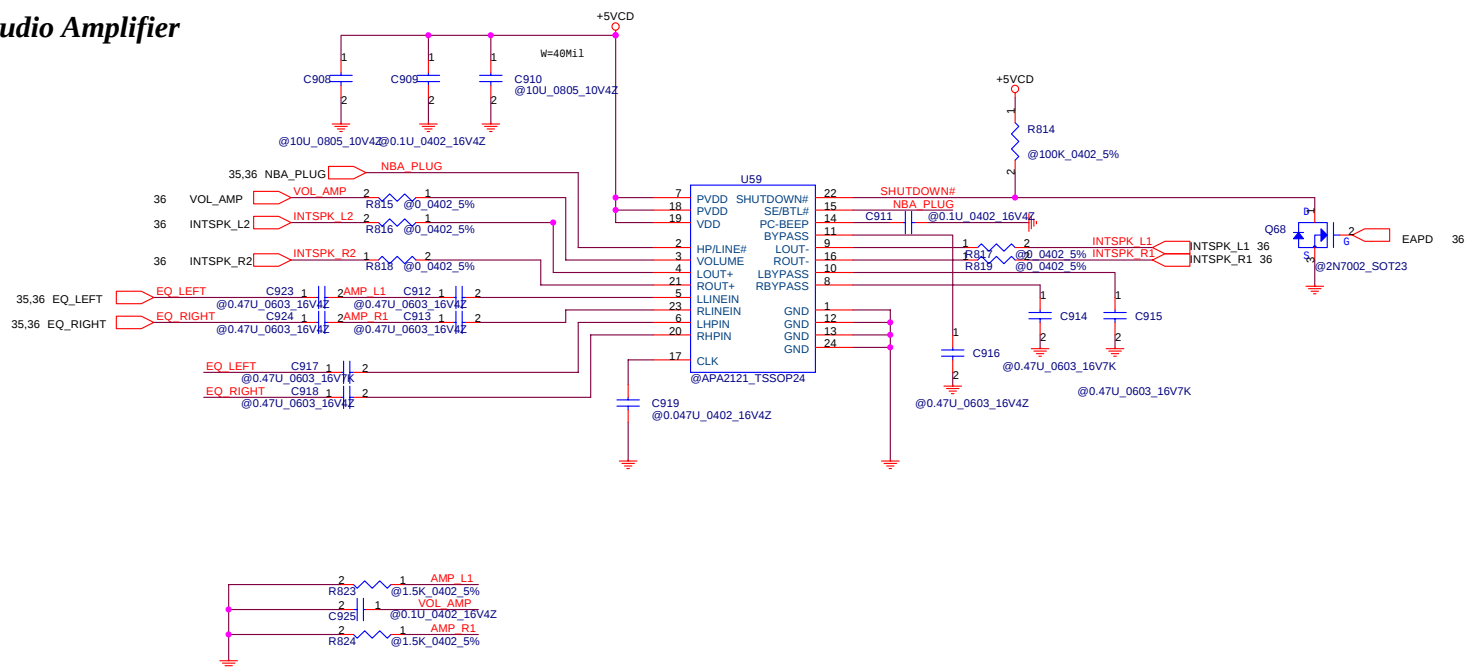
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Audio Amplifier



Compal Electronics, Inc.

Title
APA2121 Audio Amplifier

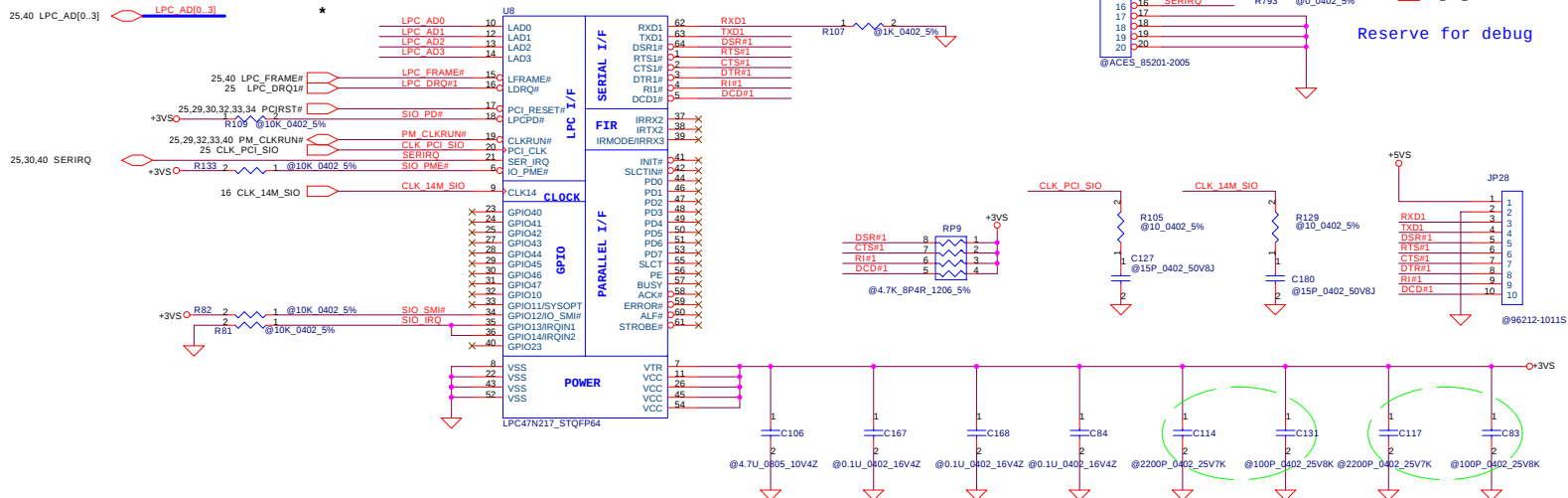
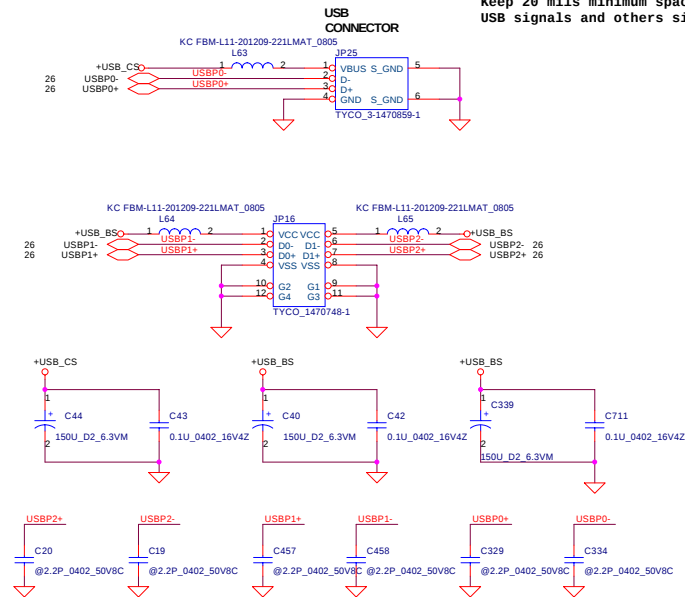
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Rev
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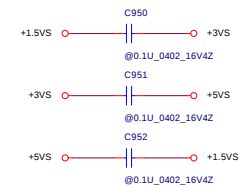
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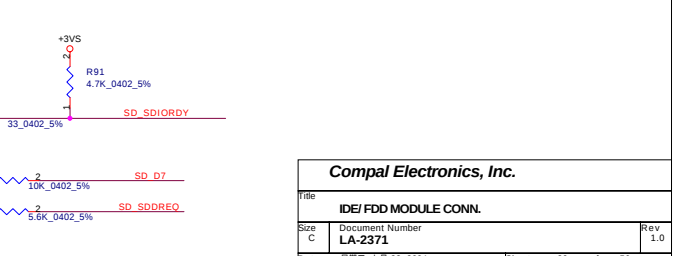
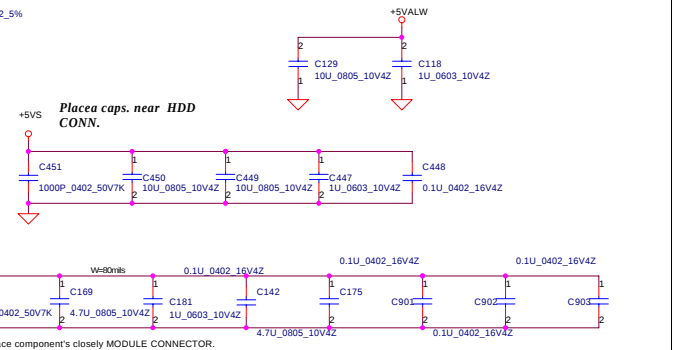
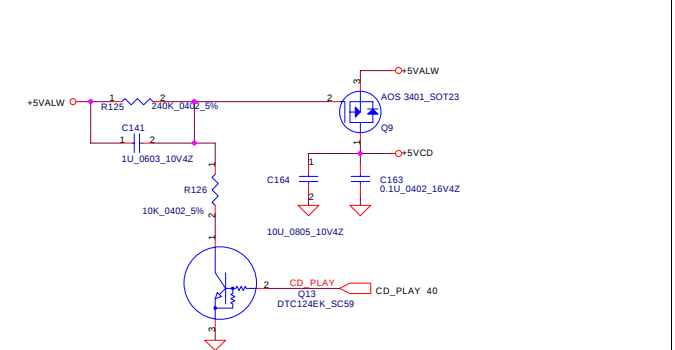
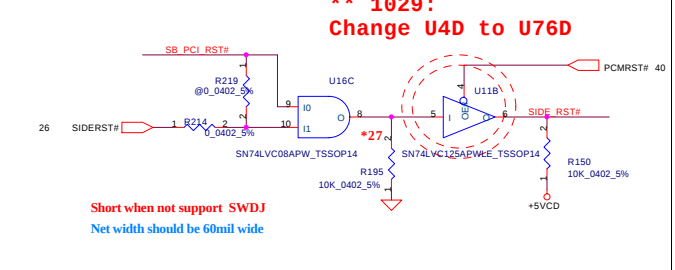
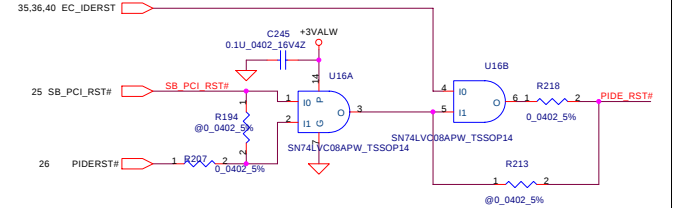
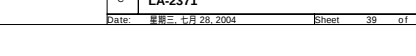
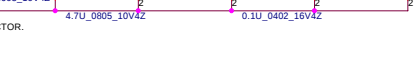
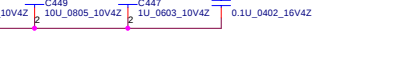
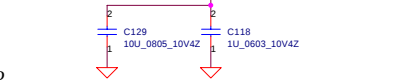
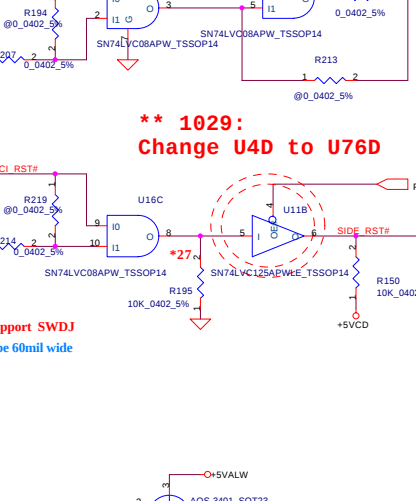
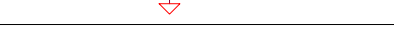
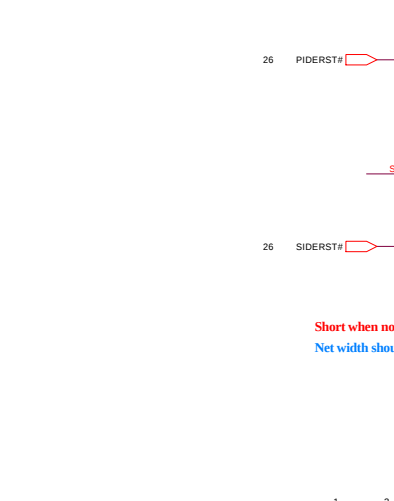
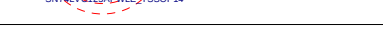
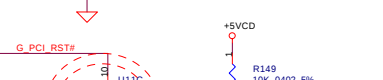
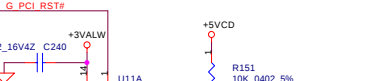
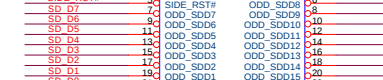
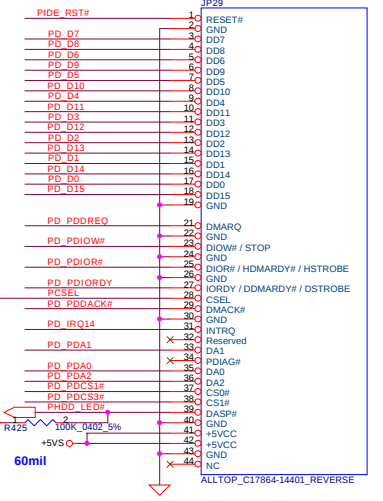
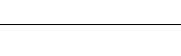
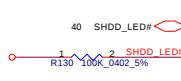
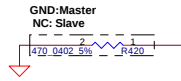
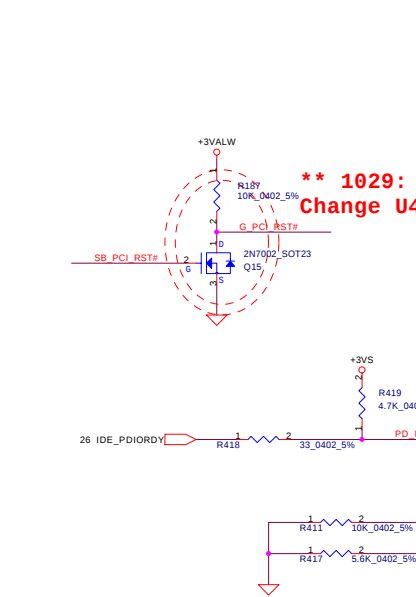
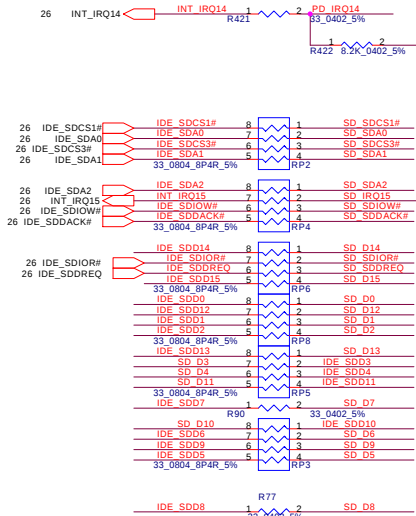
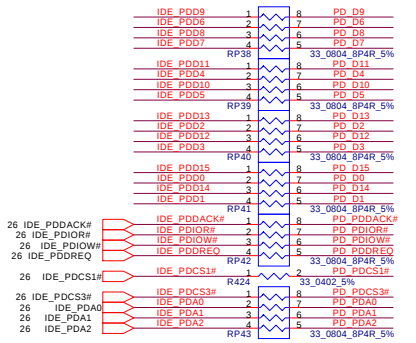
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USB
CONNECTOR
Keep 20 mils minimum spacing between
USB signals and others signals



HDD CONNECTOR



**** 1029: Change U4D to U76D**

Short when not support SWDJ
Net width should be 60mil wide

Place caps. near HDD CONN.

Place component's closely MODULE CONNECTOR.

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IDE/ FDD MODU CONN.

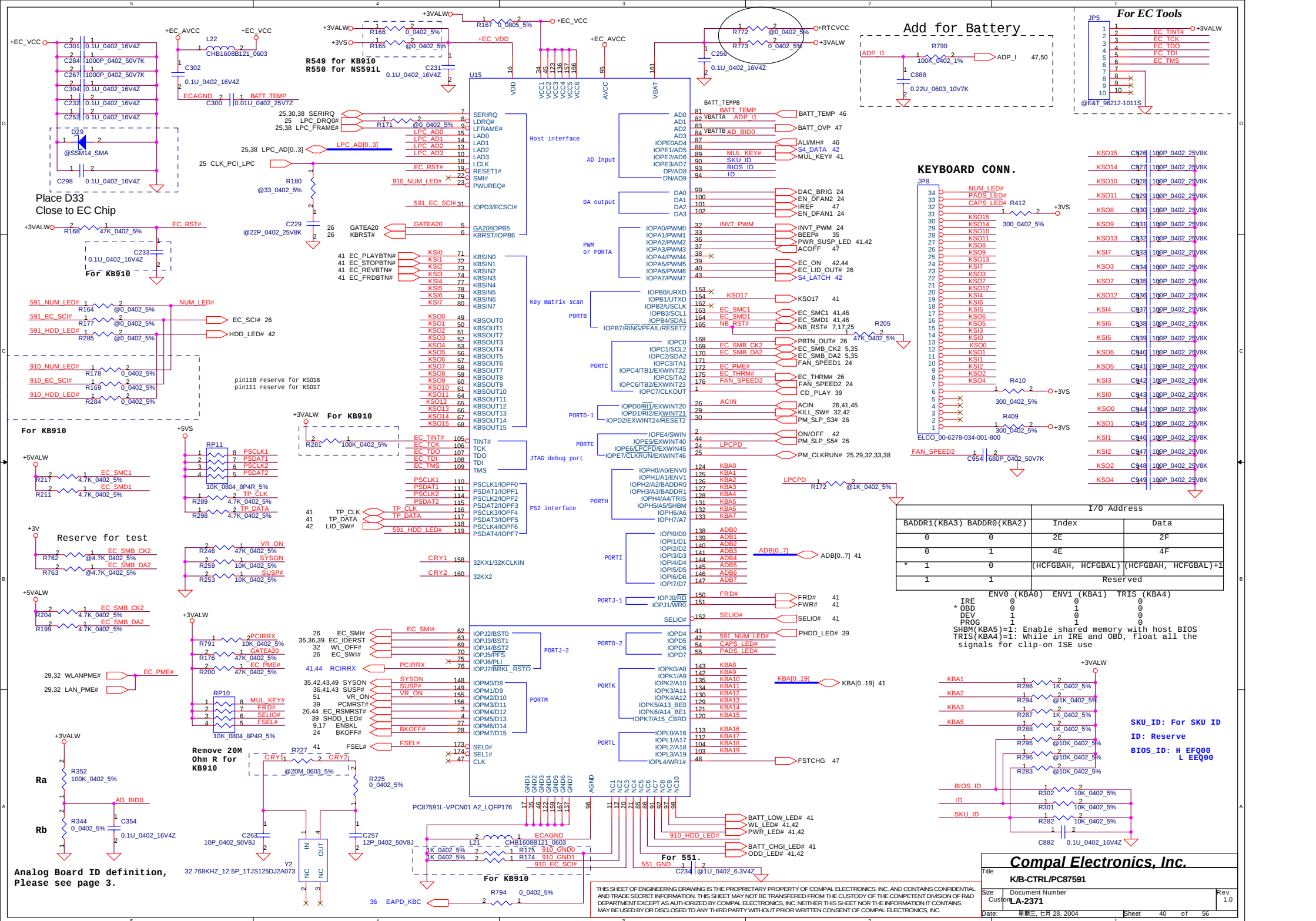
Size C

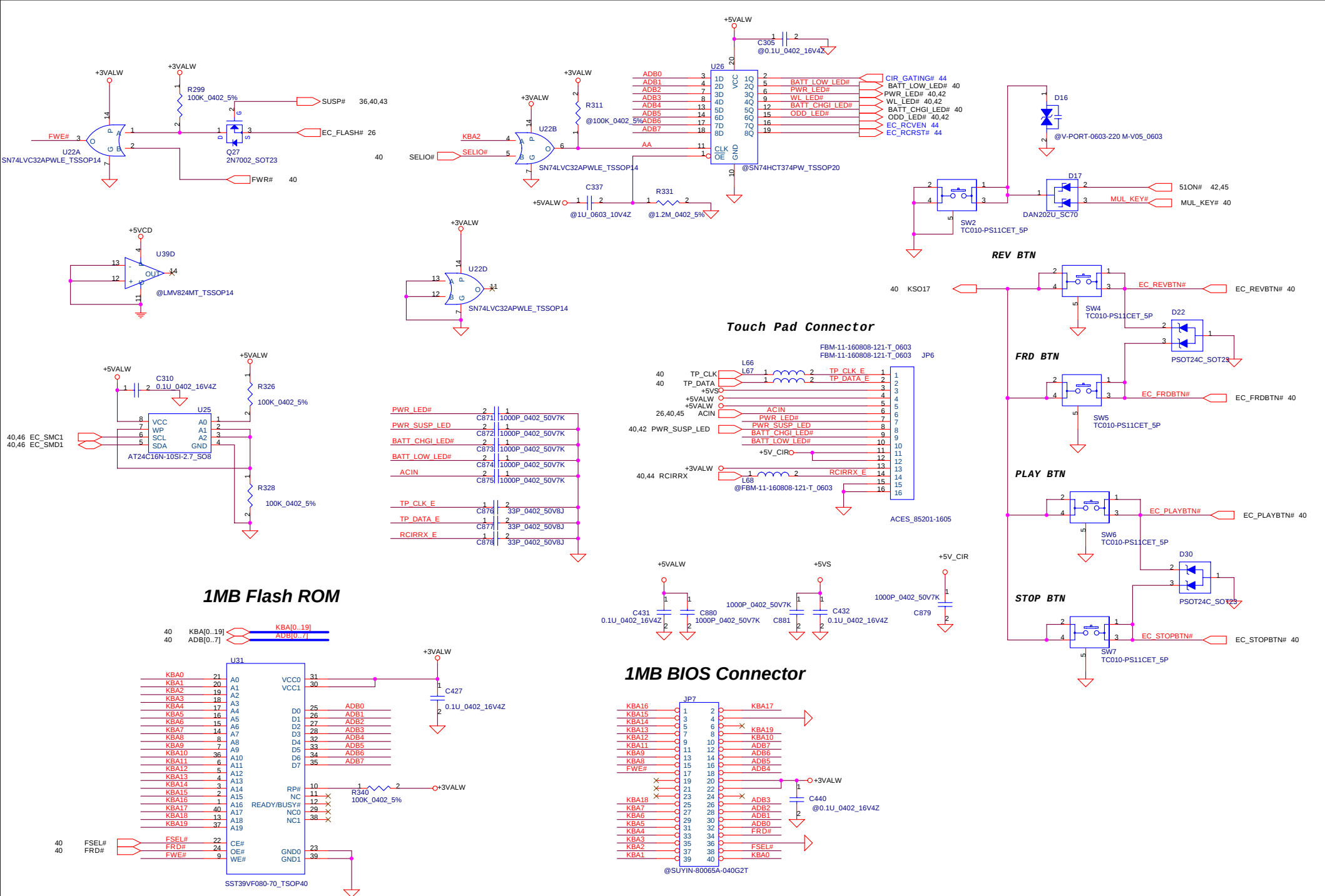
LA-2371

Date: 星期三, 七月 28, 2004

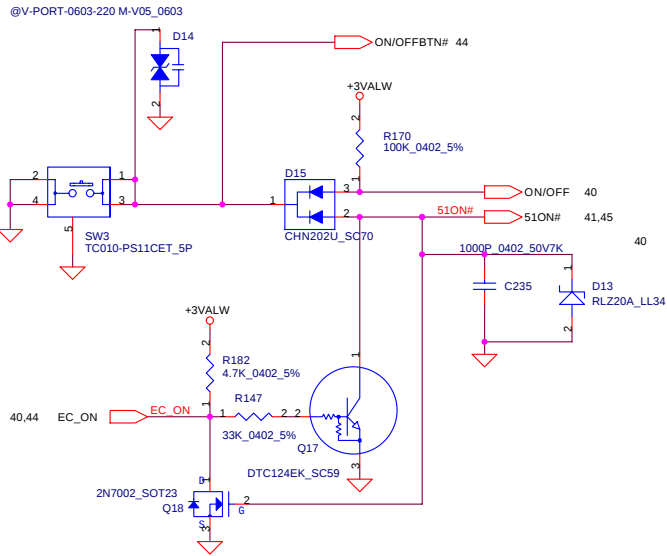
Sheet 39 of 56

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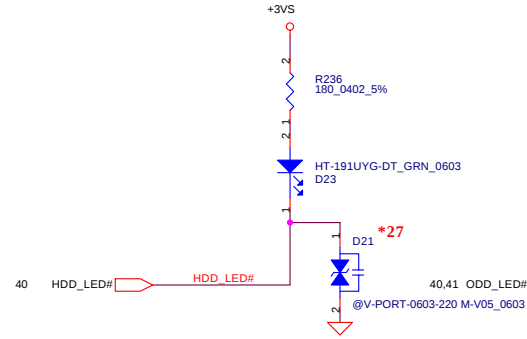




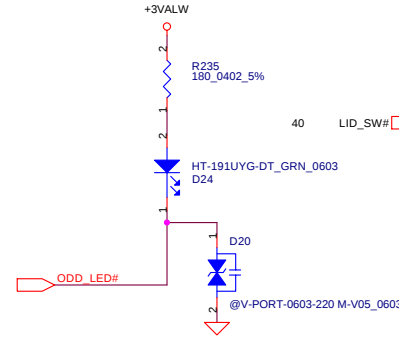
Power Button



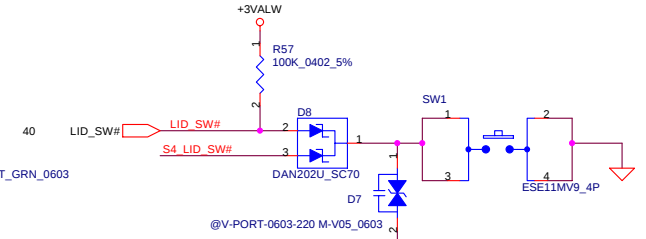
HDD LED



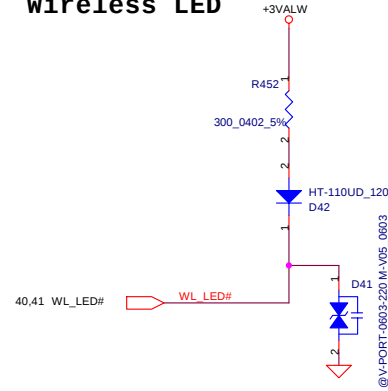
ODD LED



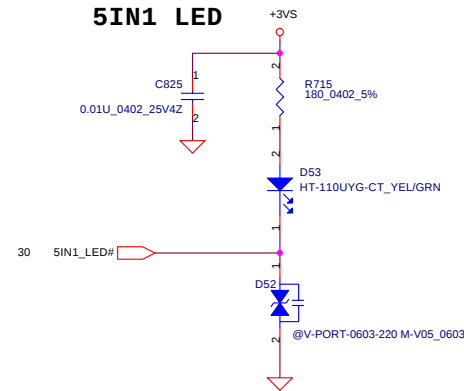
LID Switch



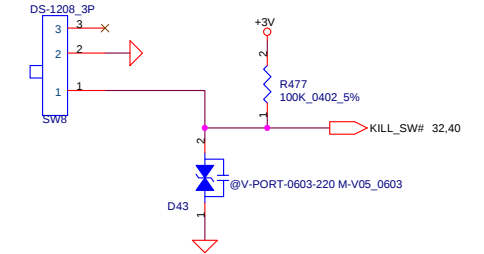
Wireless LED



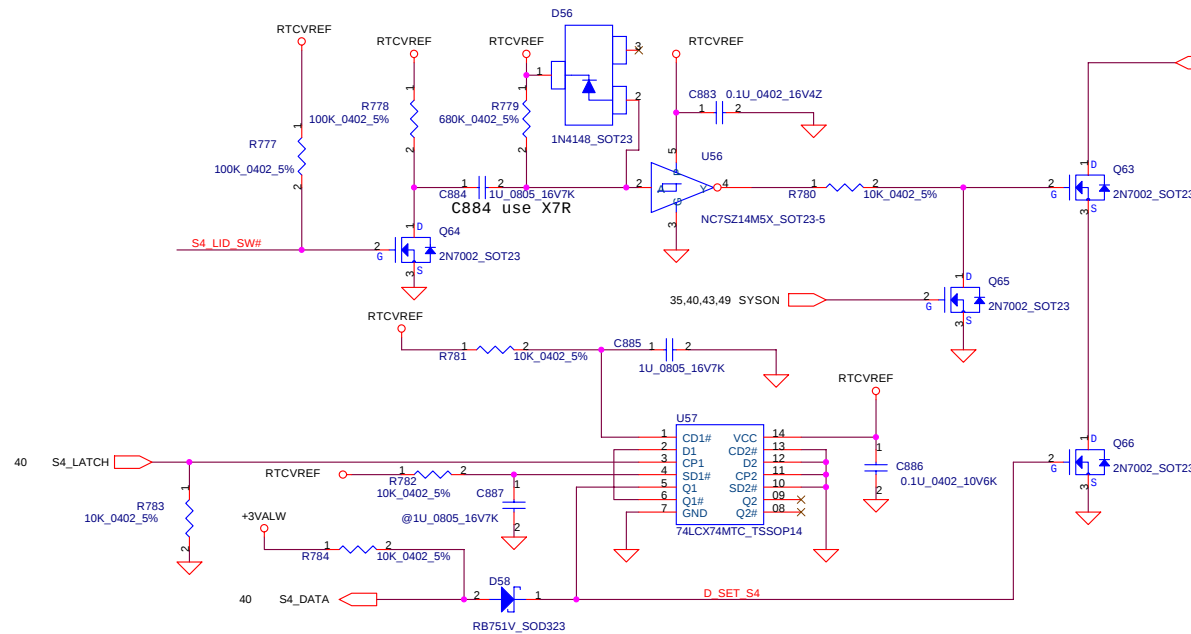
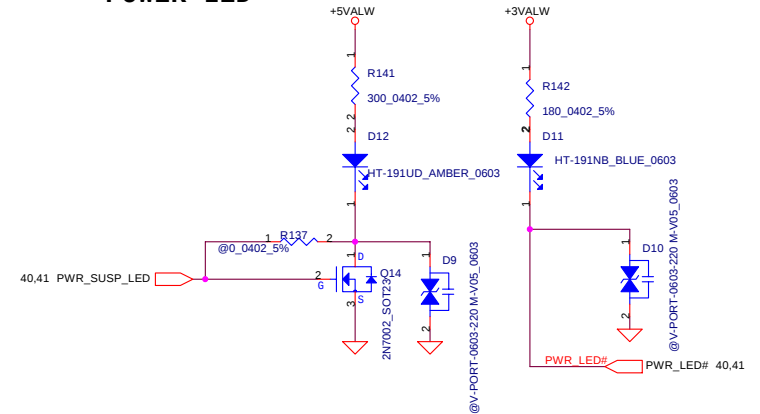
5IN1 LED



Kill Switch



POWER LED



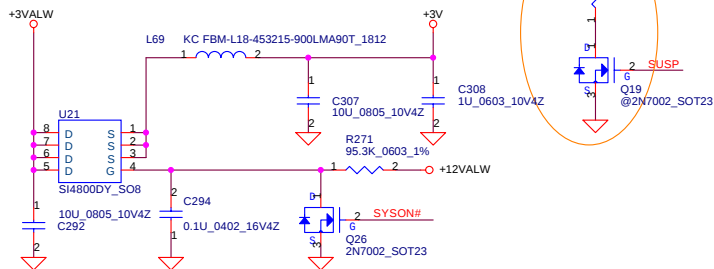
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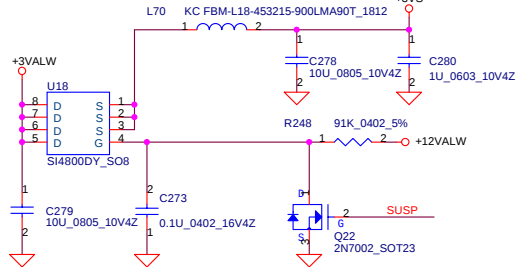
Switches & Connectors

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Custom LA-2371
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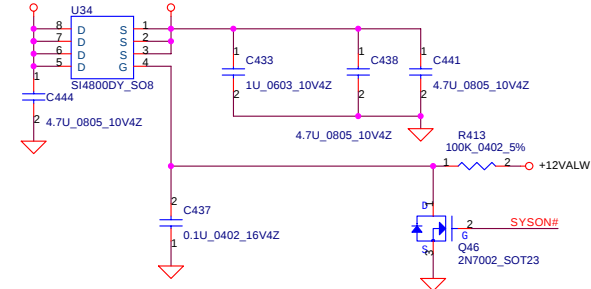
+3VALW TO +3V



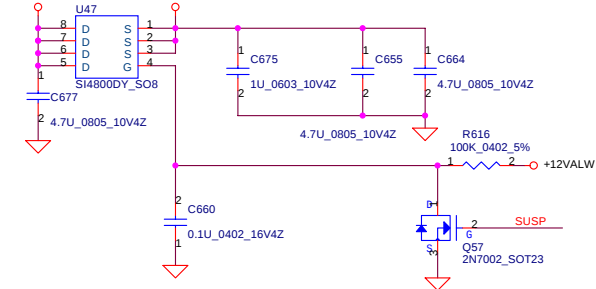
+3VALW TO +3VS



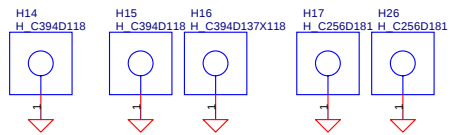
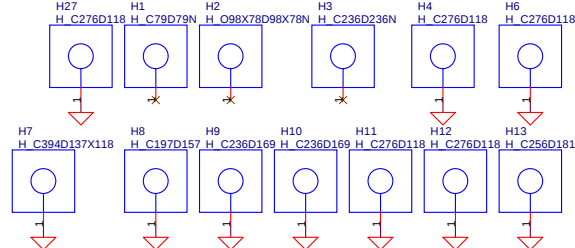
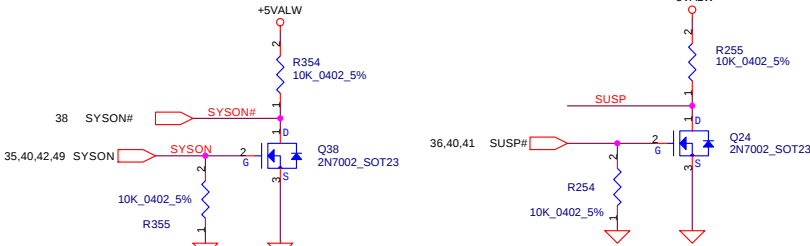
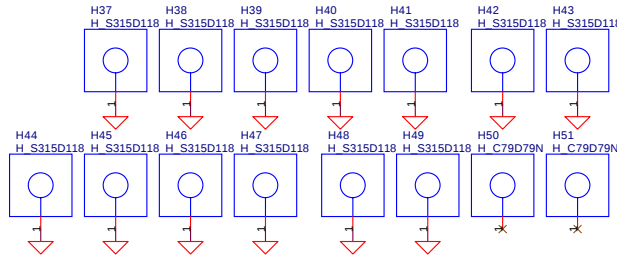
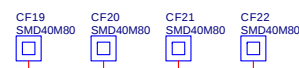
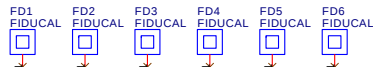
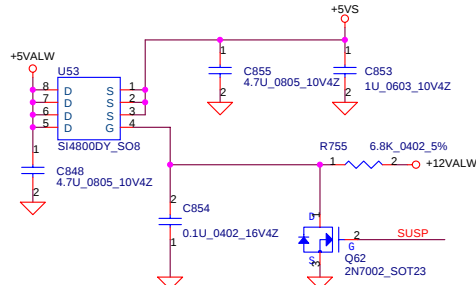
+2.5VALW TO +2.5V



+2.5V TO +2.5VS

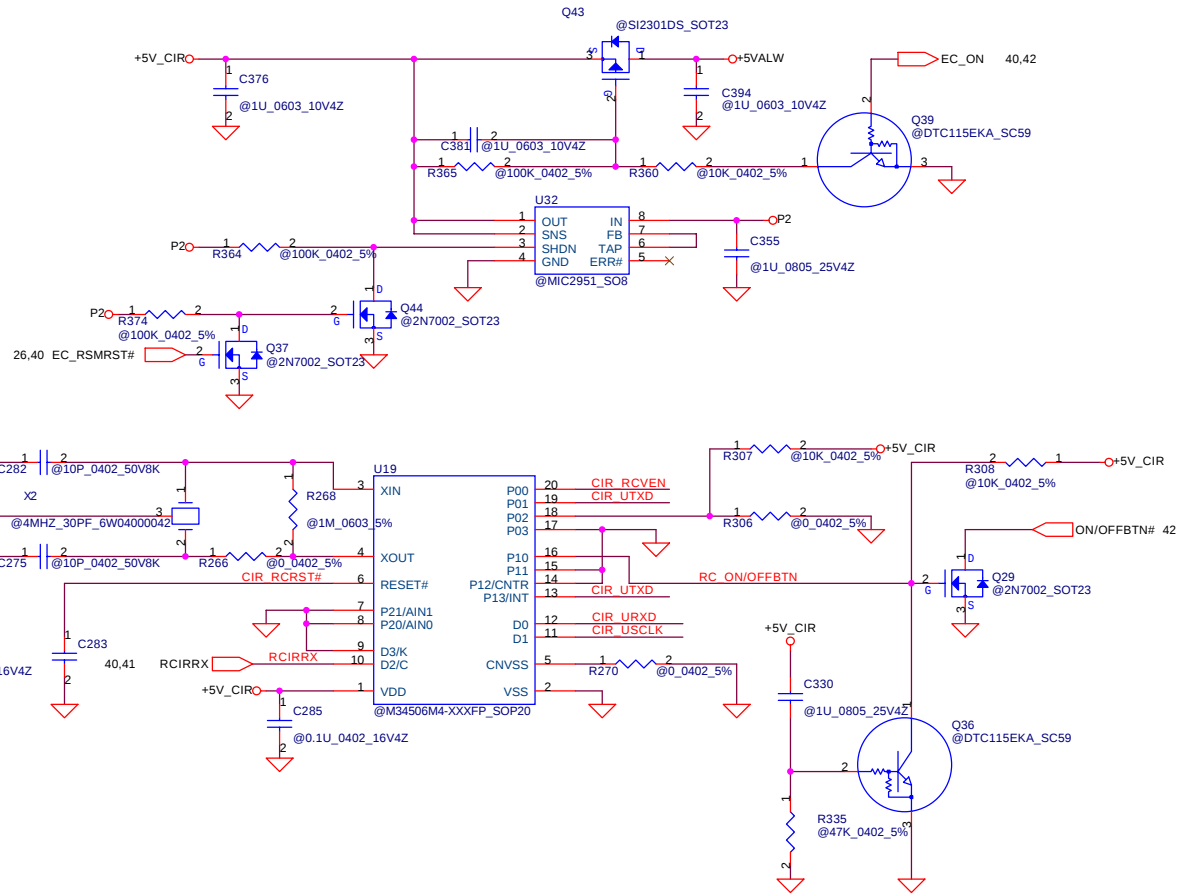
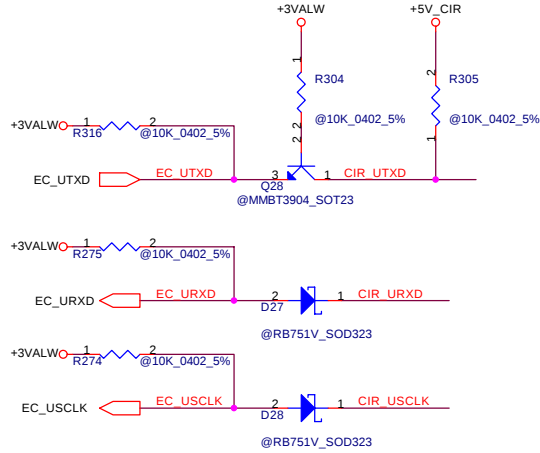
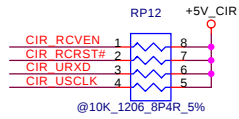


+5VALW TO +5VS

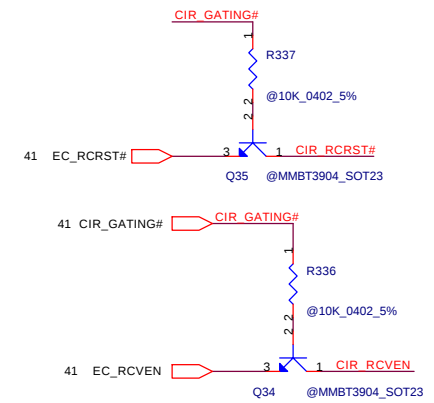
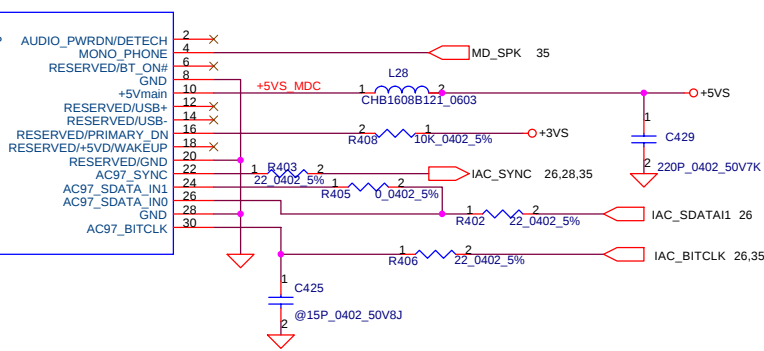
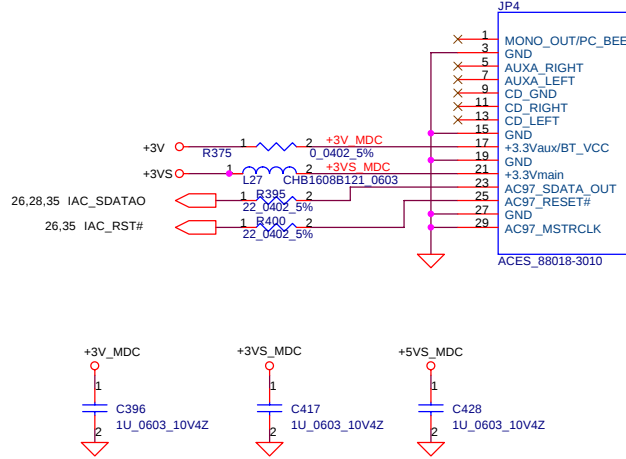


Compal Electronics, Inc.			
Title			
POWER CONTROL CKT			
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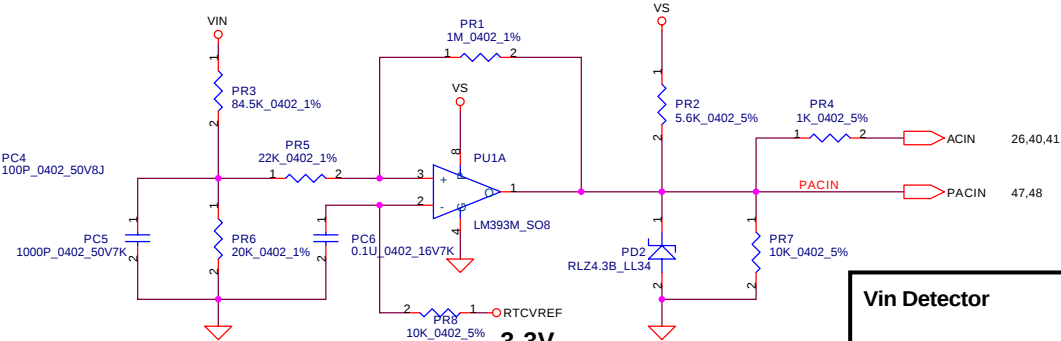


MDC CONN.

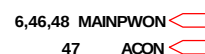
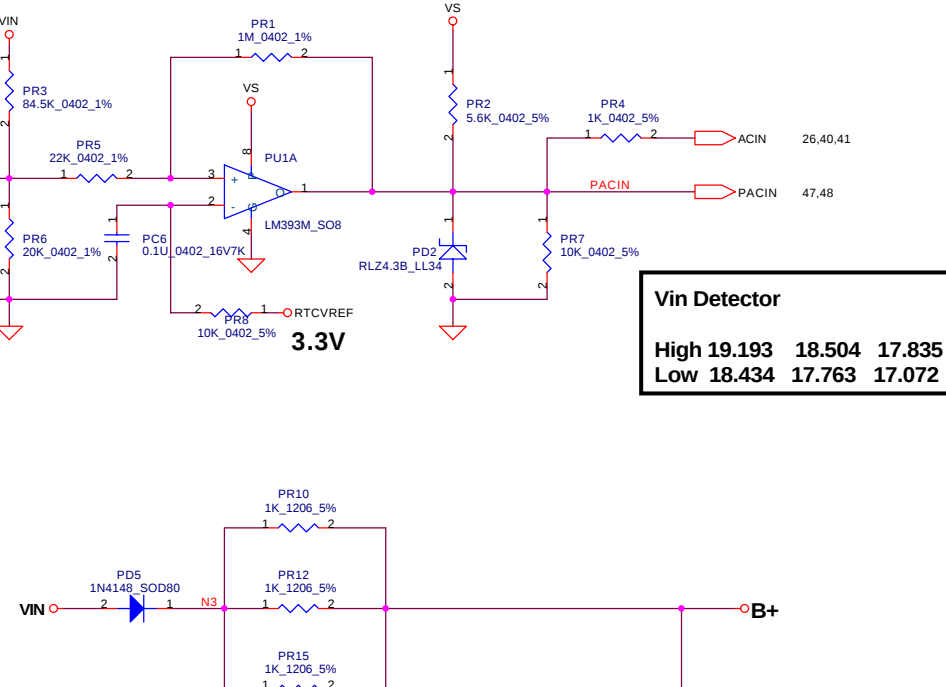


Compal Electronics, Inc.			
Title CIR & MDC			
Size B	Document Number LA-2371	Rev 1.0	
Date: 星期三, 七月 28, 2004	Sheet 44	of 56	

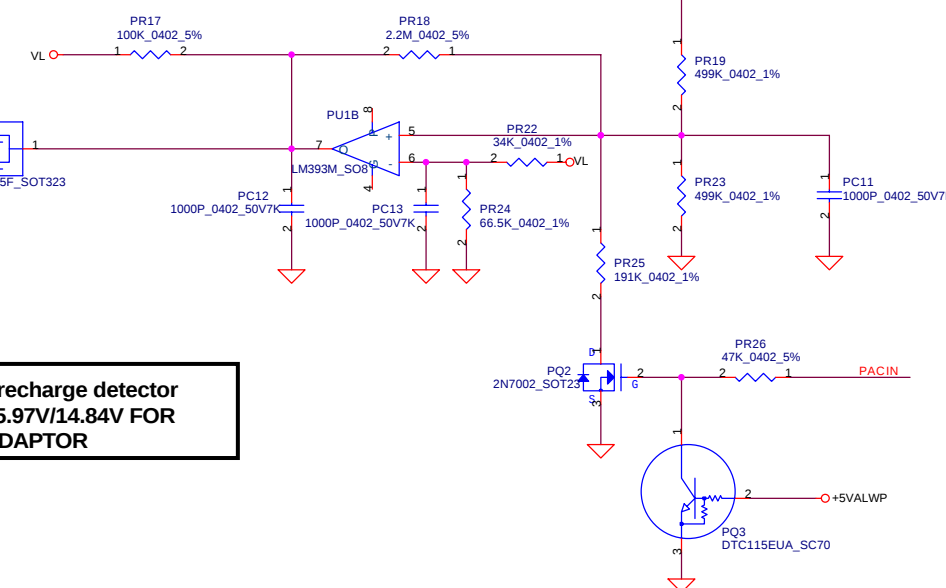
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High	19.193	18.504	17.835
Low	18.434	17.763	17.072

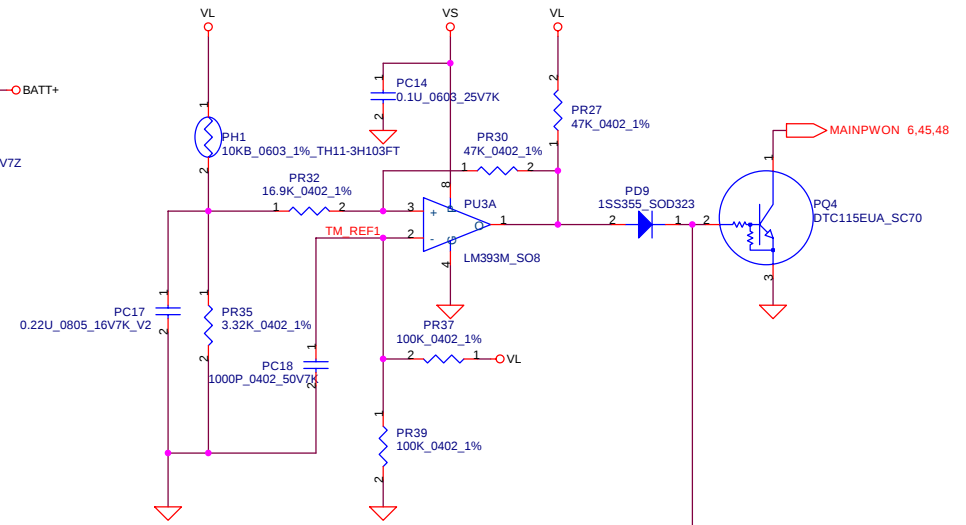


**Precharge detector
15.97V/14.84V FOR
ADAPTOR**

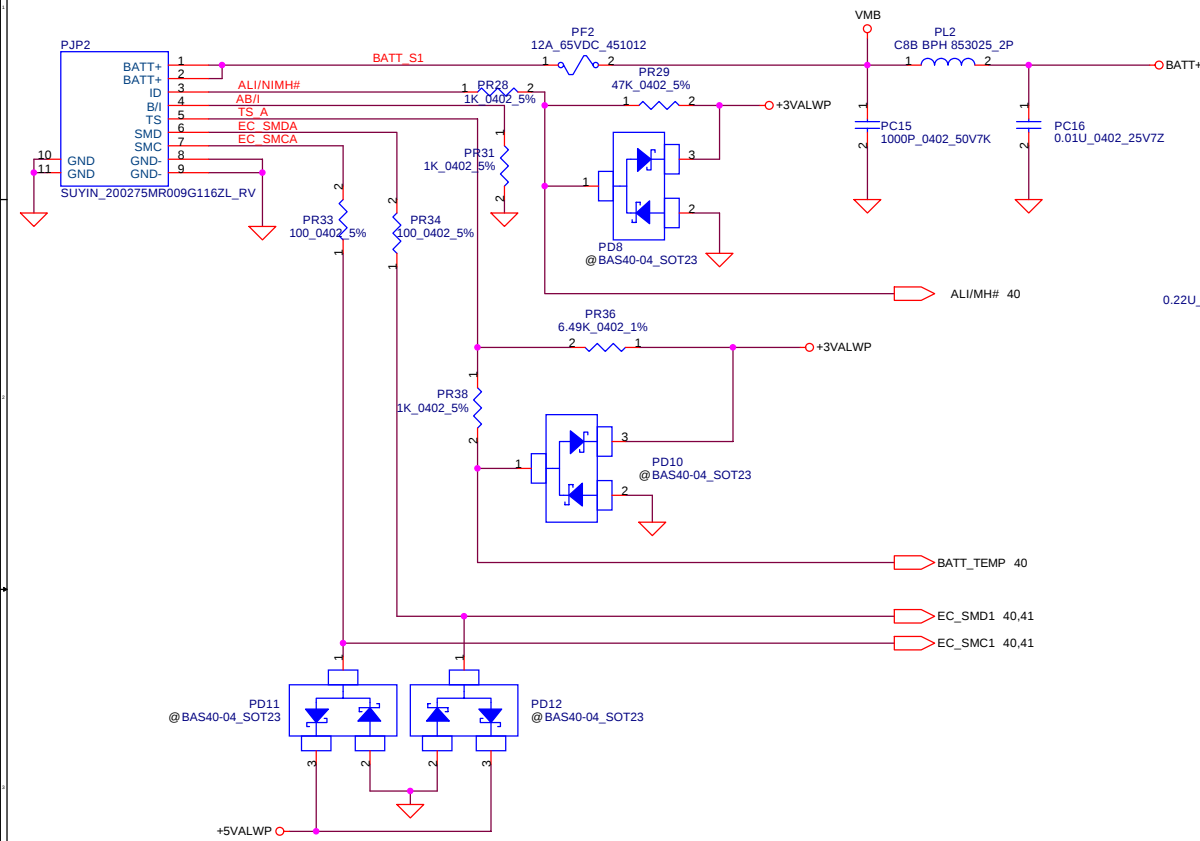
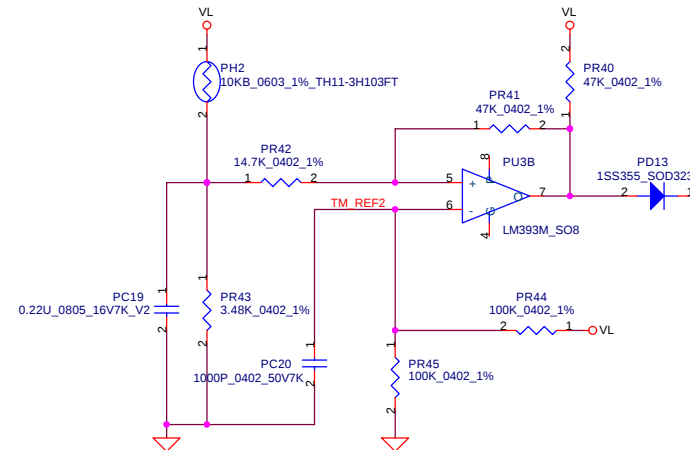


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PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C

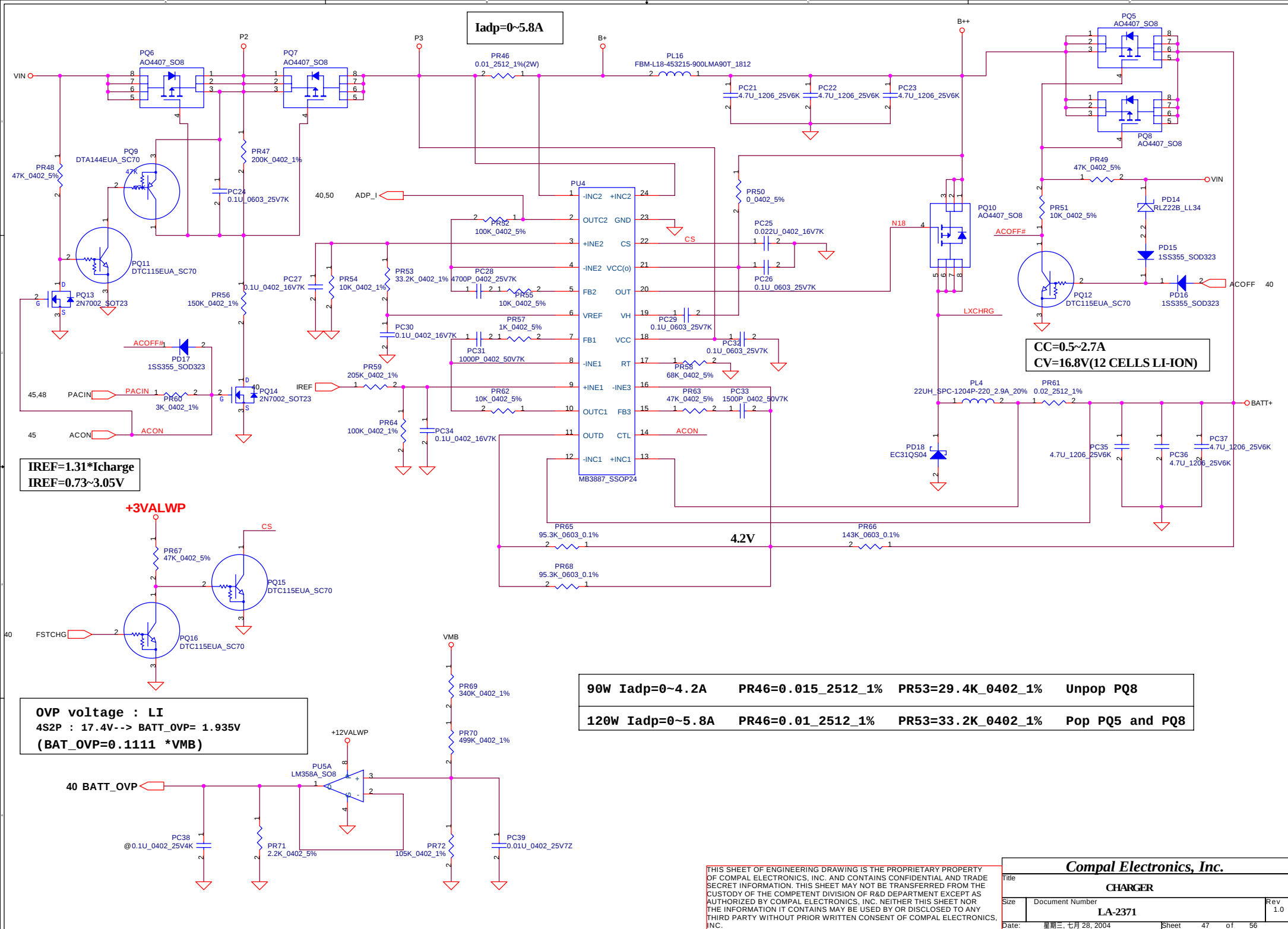


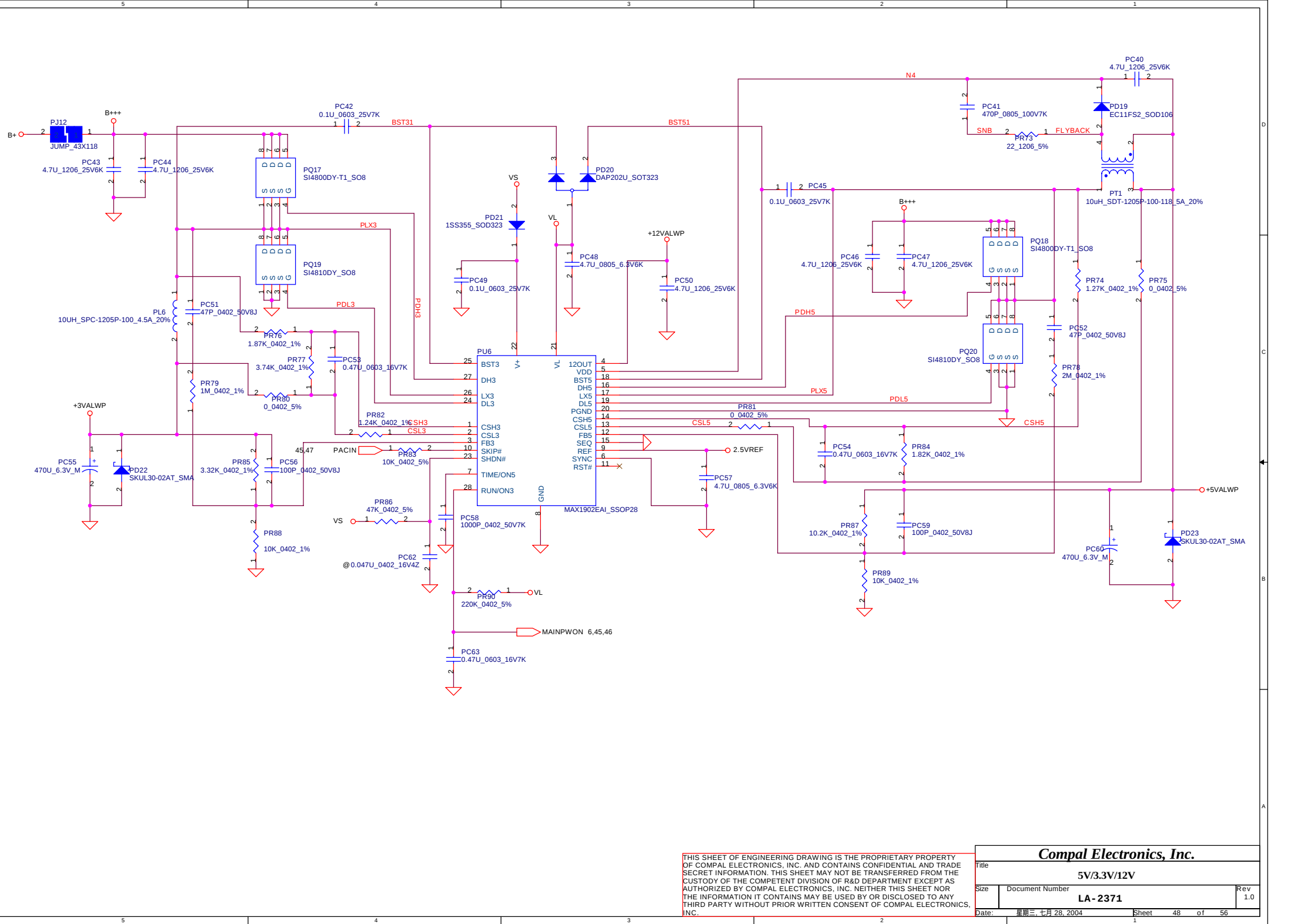
PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 45 degree C



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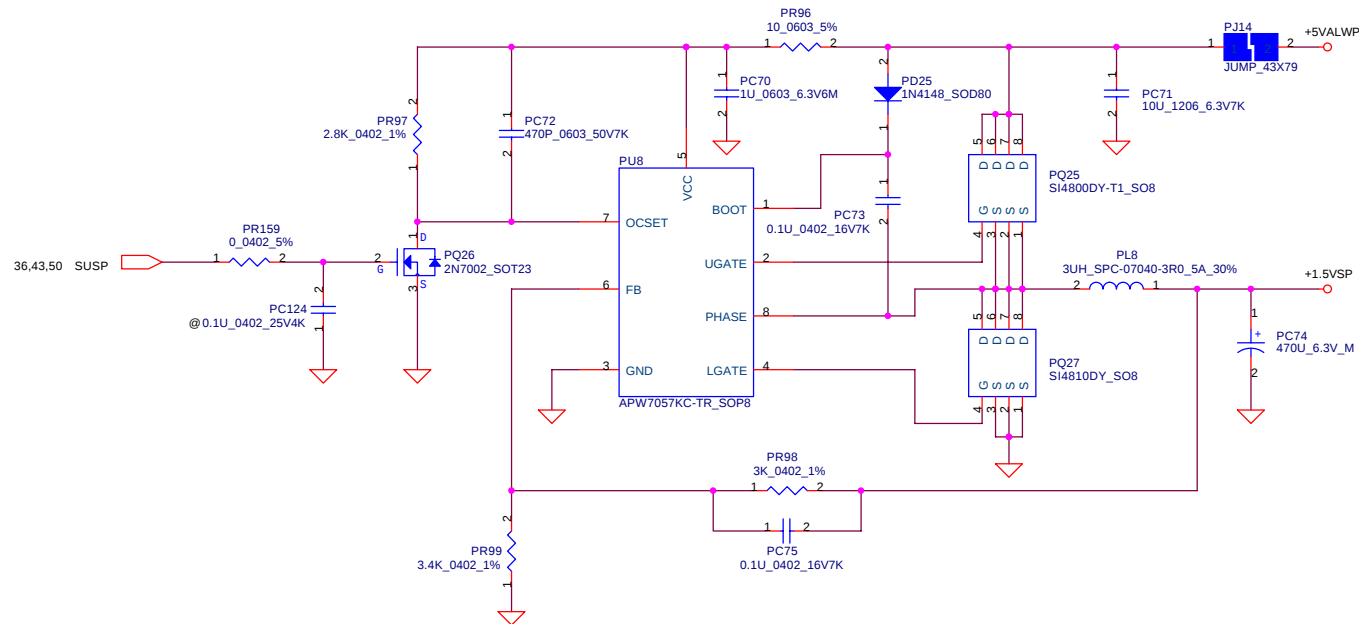
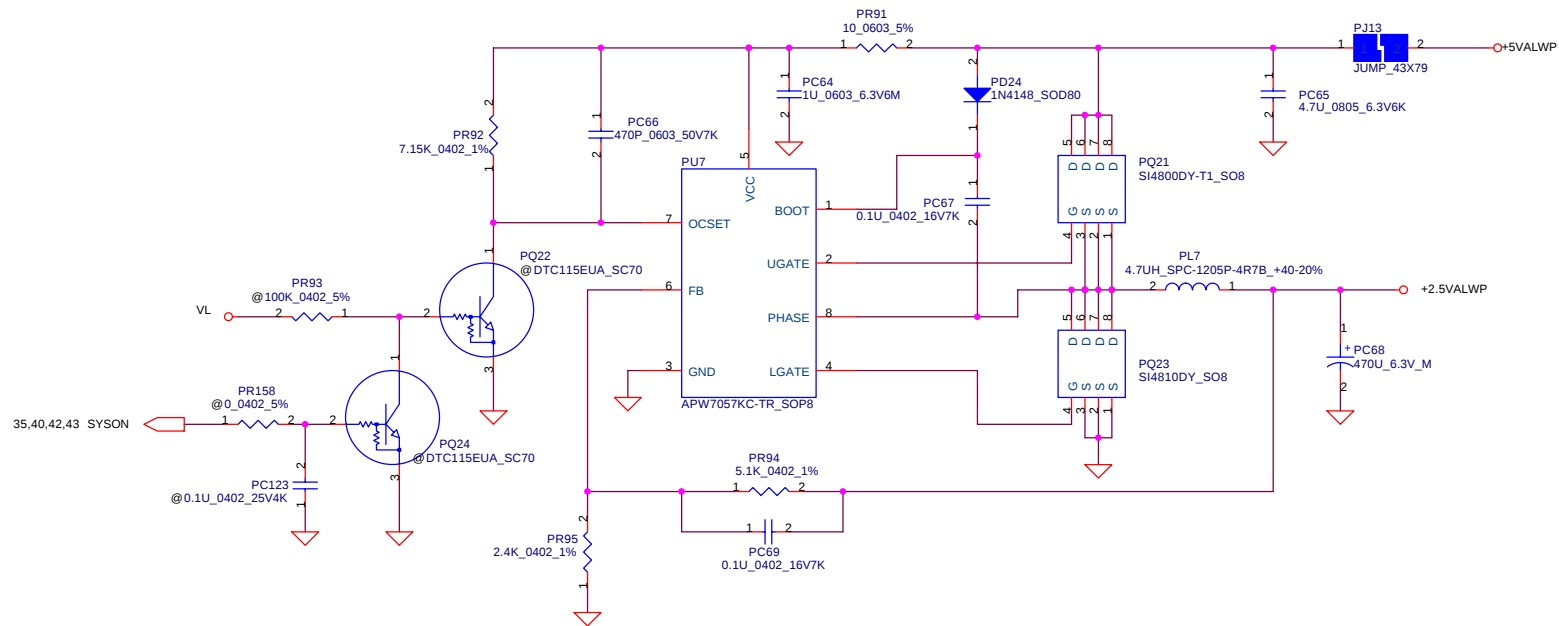
Compal Electronics, Inc.			
Title			
BATTERY CONN/OTP			
Size	Document Number	Rev	
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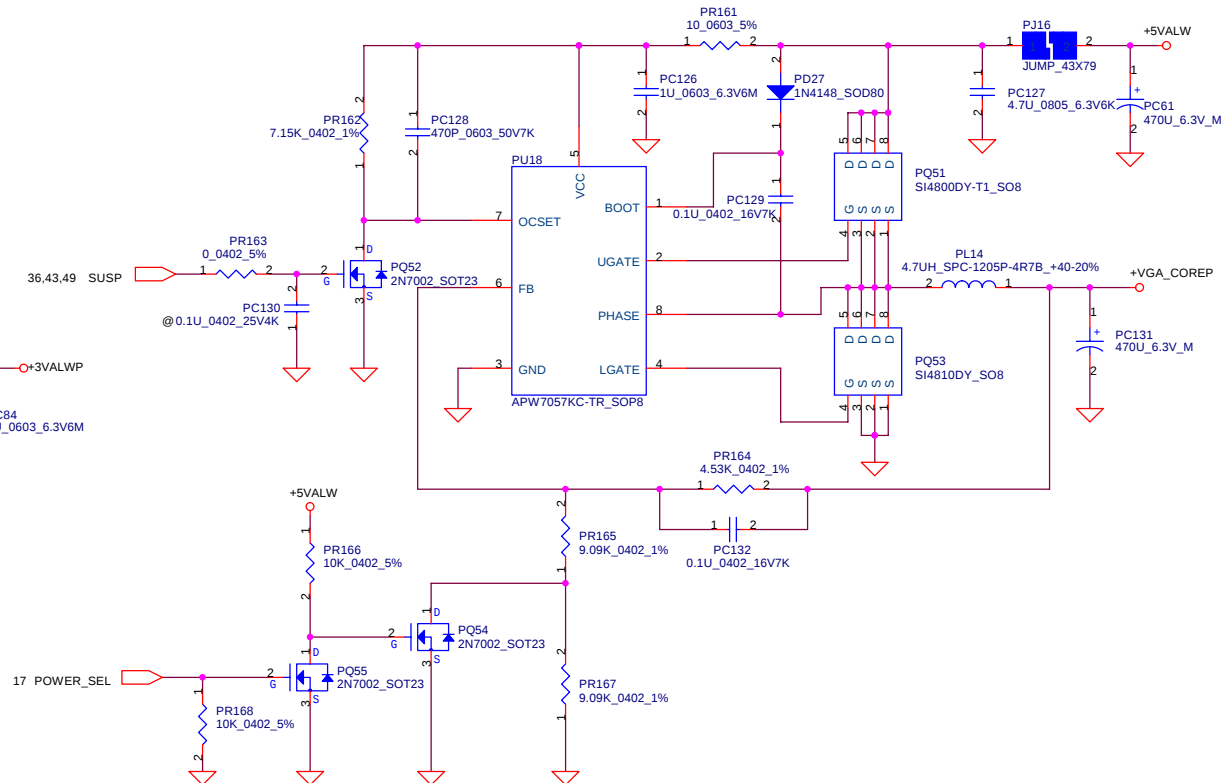
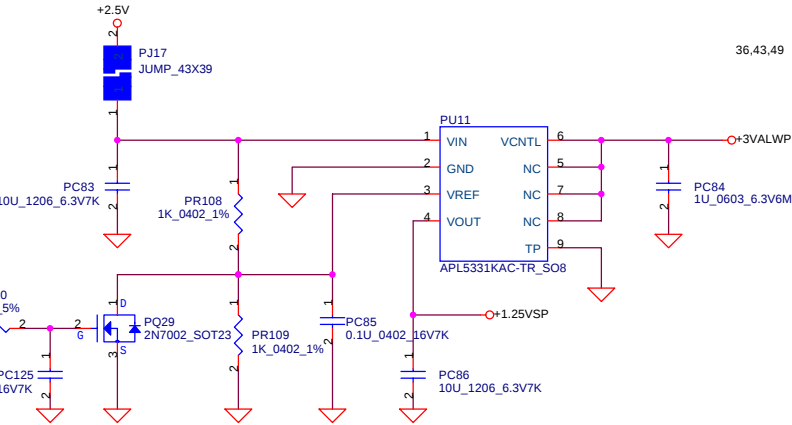
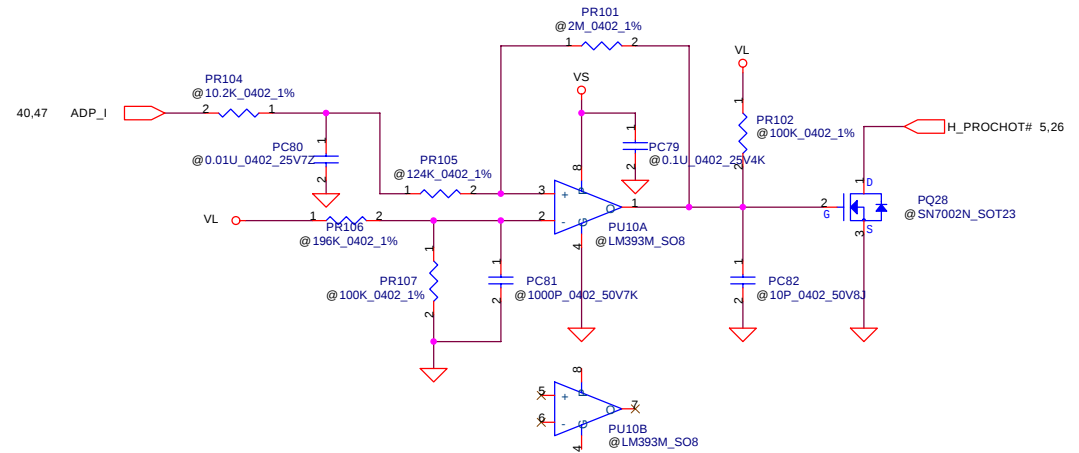
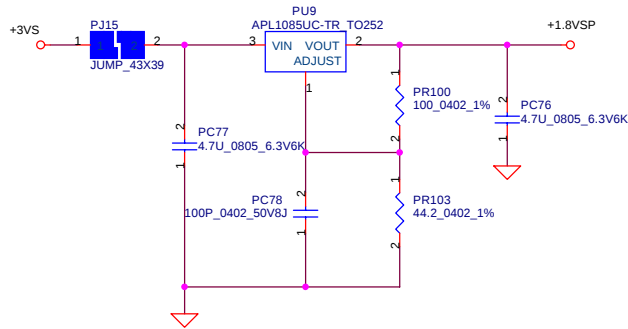
Compal Electronics, Inc.				
Title				
5V/3.3V/12V				
Size	Document Number			Rev
	LA-2371			1.0
Date:	星期三, 七月 28, 2004		Sheet	48 of 56



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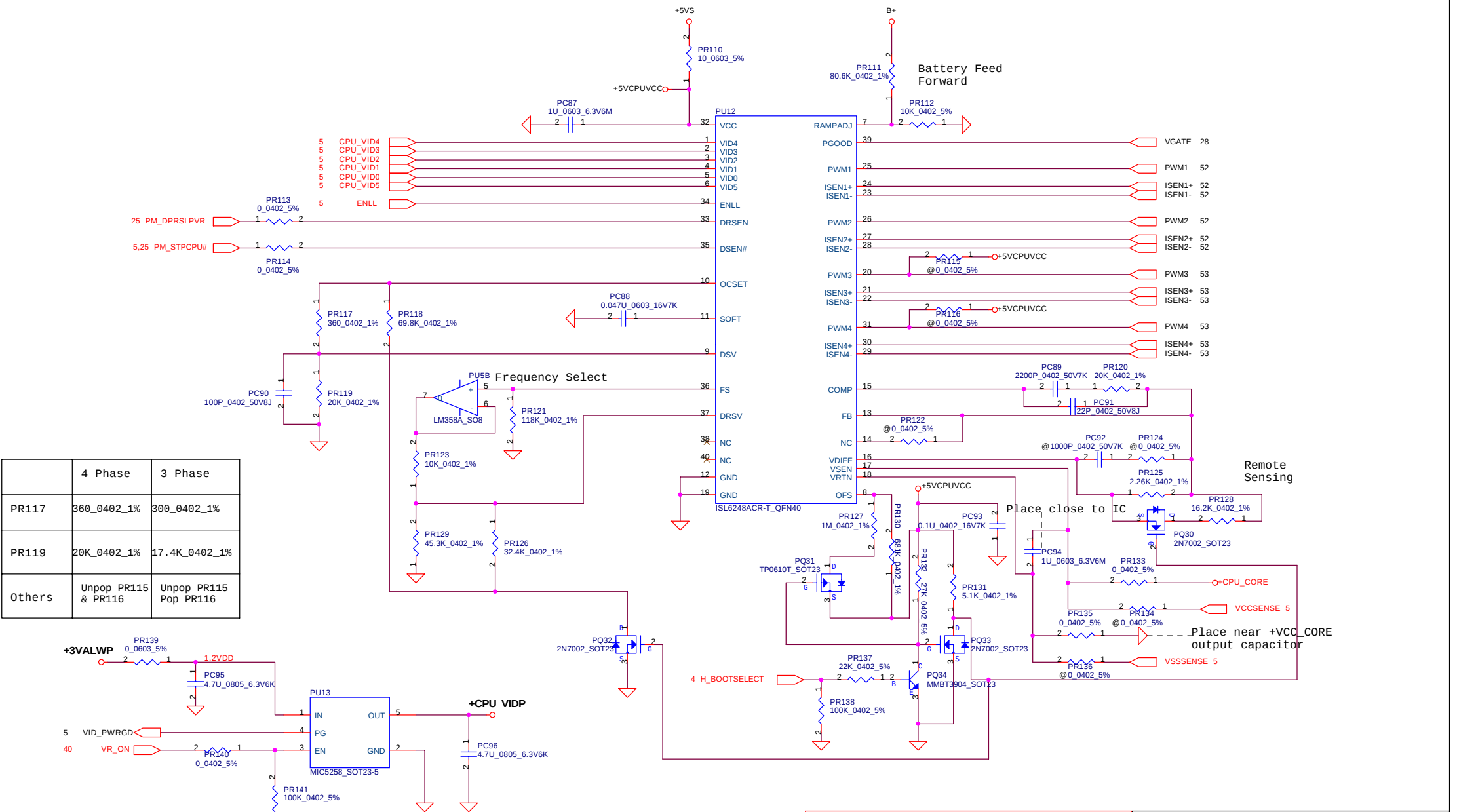
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Title		2.5V/1.5V	
Size	Document Number		Rev
	LA-2371		1.0
Date:	星期三, 七月 28, 2004	Sheet	49 of 56

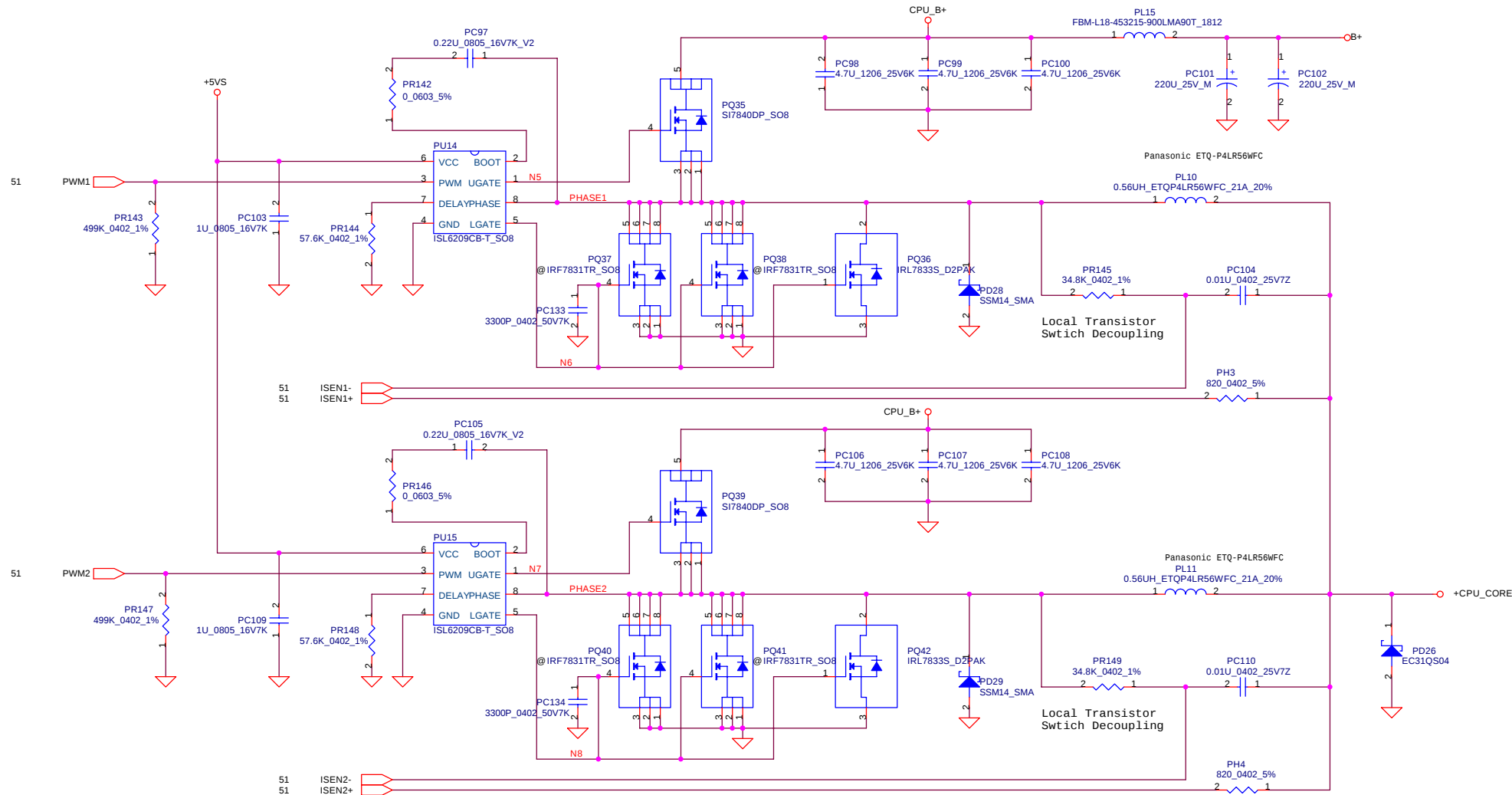
85W THROTTLING 70W REVOVERY



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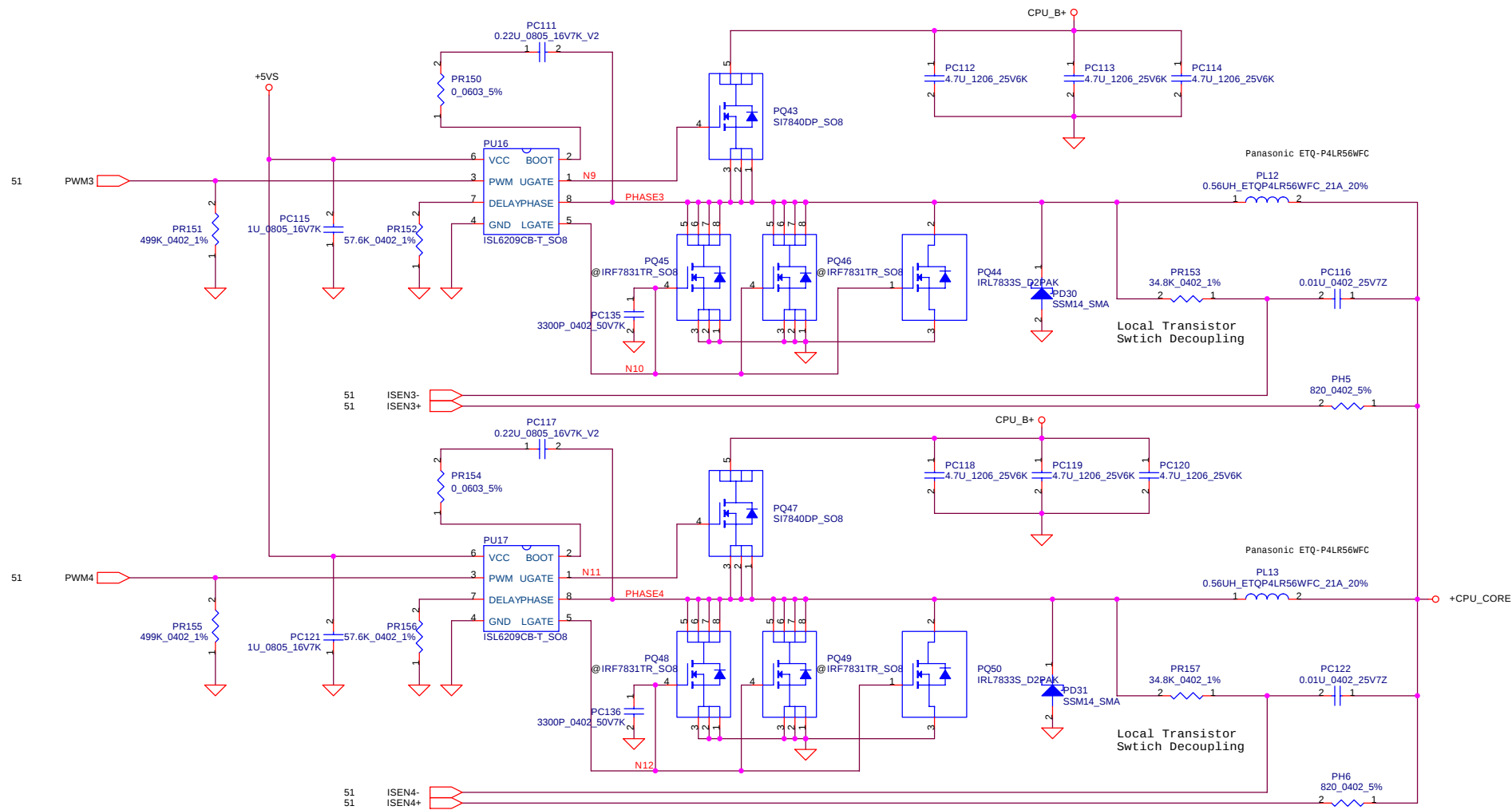
Compal Electronics, Inc.			
Title			
1.8V/PROCHOT/1.25V/VGA			
Size	Document Number		Rev
	LA-2371		1.0
Date:	星期三, 七月 28, 2004		Sheet 50 of 56





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Compal Electronics, Inc.		
Title		
CPU_CORE (1)		
Size	Document Number	Rev
	LA- 2371	1.0
Date:	星期三, 七月 28, 2004	Sheet 52 of 56



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Compal Electronics, Inc.			
Title			
CPU_CORE (2)			
Size	Document Number		Rev
	LA-2371		1.0
Date:	星期三, 七月 28, 2004		Sheet 53 of 56

POWER PIR LIST

	page	Reason for change	Modify list
DVT	45,46,49,51	Update BOM	Change PC7 form 0.022u to 0.22u(SE041224K03), PR36 from 25.5K to 6.49K(SD034649100) Change PC17,PC19 form 0.022u to 0.22u(SE030224KT1), PC71 from 4.7u to 10u(SE114106K00) Change PR130 from 340K to 681K(SD034681300) Change PC133,PC134,PC135,PC136 from 3300p to 4700p(SE75472K00)
	52	For EMI team request	Add PL15 (FBM-L18-453215-900LMA90T_1812: SM010020700)
	52	Solve noise issue	Add PC102(220u; SF22004M200)
PVT		Add 2nd source	Add 2nd source
		For common part with H/W	Change PQ13,PQ14,PQ2,PQ26,PQ29,PQ30,PQ32,PQ33,PQ52,PQ54,PQ55 from SB570020500 to SB7700200T5
	45,47	For common part	Change PD1 from EC10QS04(SC10QS041T4) to SSM14(SCSSSM14000) Change PD18 from RB051L(SC1B051L000) to EC31QS04(SC11QS04000)
	48	To decrease 3V/5V negative voltage	Change PD22,PD23 from SSM14(SCSSSM14000) to SKUL30-02AT(SCSKUL30000)

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P.40 Change R175 and R176 from 0 to 1K ohm
Add @ in R172

P.42 Modify S4 resume circuit

7/27 Write by Timo Teng

P.24 R31,R34,R32,R33 from 75_0402_5% to 1%

P.31 Add R825
Change 789 from 43K to 10K

P.36 Change JP10 and JP11 from ACES 85204-0200 to ACES 85205-0200

P.40 Add C954 at pin176 of U15

7/28 Write by Timo Teng

P.30 Add R826
Change R721 from 33 to 22 ohm

P.30 Del R743

For solve KB910 into test mode
For LPDPC doesn't be used
For solve KB910 into test mode

For solve power switch ripple
For ME request
For FAN2 test Fail

For SD Card Function